Journal of the Institute of Circuit Technology

2010 Events

2nd November	17.00 Evening Seminar, Darlington
9th - 12th November	*Electronica 2010, Munich International Fair, Germany*

2011 Events

25th January	*EIPC Road Show on Reliability at Enthone Ltd., Woking*
1st February	15.30 Afternoon facilities tour of CCE Europe 17.00 Evening Seminar, Chimney House Hotel, Sandbach supported by CCE Europe
1st March	17.00 Evening Seminar, Arundel, Norfolk Arms Hotel
11th April - 14th April	**ICT Annual Foundation Course** , Loughborough University bill.wilkie@InstCT.org
1st June	**ICT 37th Annual Symposium**, organised in collaboration with the Sonochemistry Centre, at the Coventry University Techno Centre supported by Ventec-Europe bill.wilkie@InstCT.org
7th September	15.00 Facility Tour of Spirit Circuits, followed by afternoon tea. 17.00 Evening Seminar bill.wilkie@InstCT.org Newtown House Hotel, Hayling Island http://www.newtownhouse.co.uk/ supported by Spirit Circuits.

Contents

vol.4 no.2 1st April 2011

Editorial

Tom Parker – the Benefits of ICT Membership

With an association with the ICT that stretches back more then three decades, there can be few better placed to give an informed opinion of its benefits than CC Electronics Europe (CCEE) customer technical and quality manager, Tom Parker.

Tom recently became a member of the ICT Council but prior to that appointment the amiable Welshman had been a regular attendee at the organisation's numerous seminars, technical forums and open days. He comments: "I must have been a guest or delegate at more ICT events than I care to remember! However, I can honestly say that every one of them gave me something to go away with.

"Whether it's a new contact through a networking opportunity, learning something new or feeling like you've helped someone else to get a clearer picture about a problem they might have been struggling with themselves, every event has produced something worthwhile."

The ICT has always taken great pride in providing its members and guest delegates with pertinent seminars and technical forums that have provided a range of sage advice, news of technological advancements or in-depth detail about specific subject matters. Tom continues: "The scope the ICT gives for technical exchange is immense.

"From the content of the seminars themselves to the information and detail you can pick up from little more than informal conversations, the knowledge transfer has always been a key feature and major benefit of being a member.

The membership boasts some highly experienced professionals and if anyone ever thinks they know it all, attendance at just one event will soon make them realise that nothing could be further from the truth.

"The quality of the multi-channel flow is exceptional and when I pause for a moment and consider the generic business advice I've received over the years, I can say with some confidence that the organisation has played a big part in helping to shape my own career.

"Indeed, we recently held an Open Day at CCEE and even then, after over 30 years in the industry, I still went away feeling that I had learned something that could have a positive impact on our business."

The provision of an ongoing Technical Forum on the ICT website, where people can log-on anonymously and ask for help and advice, the organisation always does its level best to facilitate the exchange of knowledge.

"After over three decades of making use of the organisation, I can genuinely say that I get more out of it now than I ever have and would urge anyone with a thirst for knowledge and professional development to come along to an event near them as soon as they can to see for themselves just how beneficial membership can be."

Tom Parker
ICT Council Member

Membership

New members notified by the Membership Secretary

Associate (A.Inst.C.T.)

10180 Uvie Gordon

Member (M.Inst.C.T.)

10168 Andy Greasley
10169 Victor Lau
10170 Michael Bingham
10171 Lee Lloyd
10173 Chris Kenward
10174 George Wheadon
10175 Martin Randall
10176 Mark Knowlton
10177 Andy Prince
10178 Peter Dobromylski
10179 Andy Roberts
10181 Jonathon Griffiths

Fellow (F.Inst.C.T.)

10172 Steve Driver

Corrections and Clarifications

It is the policy of the Journal to correct errors in its next issue.
Please send corrections to : -
E-mail : bruce.rout@btinternet.com

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ASPIS
– a new multi-partner research project to enhance the performance of nickel-gold solderable finishes

A new European research project has recently commenced in order to undertake a multi-faceted approach for developing novel and improved nickel-gold solderable finishes.

The three year project is known as ASPIS, which is an abbreviation of Advanced Surface Protection for Improved Reliability PCB Systems, and it is being supported via the European Commission's 7th Framework programme under the FP7-SME AG-2008-2 call.

It is a 'Research for SME Associations' project that has twelve partners from across Europe, including four key research organisations who will undertake much of the research programme on behalf of the project's SME members.

There are two UK-based research providers, namely ITRI Ltd and the University of Leicester, along with TNO from Holland and the Center for Physical Sciences and Technology in Lithuania.

The other partners represent a wide cross section of organisations from the PCB sector that cover the whole of the requisite industry supply chain. These organisations are

Atotech GmbH,
Graphic plc,
Merlin Circuits Technology Ltd,
Scionix Ltd,
Somacis S.p.a
Global Interconnect Services.

In addition, the European Institute of Printed Circuits (EIPC) and the Institute of Circuit Technology (ICT) are partners in the project and they are undertaking the dissemination activities to bring the technology developed to the attention of the PCB industry in the UK, the rest of Europe and further afield.

The project is being managed by the Institute of Circuit Technology

The ASPIS project has a focus on nickel-gold (ENIG) solderable finishes for PCBs, and will develop new, more reliable materials and processes in order to address the key issues such as 'black pad' that have been a cause of concern for many years to both PCB fabricators and end users.

One of the key factors impacting the overall reliability of electronic assemblies is the quality of the solder joints that connect components to a circuit board and a critical factor in determining this reliability is the solderable finish that is applied to the board.

The de facto standard choice of PCB solderable finish for high reliability, high value electronics is nickel-gold. This utilises an undercoat of electroless nickel which is deposited on to the copper of the PCB and on top of which is a thin coating of immersion plated gold.

Globally, the market share of ENIG in the PCB industry as a whole is estimated at 15% by surface area of PCB manufactured. However, in terms of the value of the resulting products, the market share is considerably higher.

For the EU's electronics manufacturers, which are increasingly producing high value and high reliability products, the importance of ENIG is much greater.

ENIG has several key advantages over other types of PCB solderable finishes. These advantages are highly significant as, despite the higher price of ENIG over other alternatives, it is the preferred choice of finish for many applications.

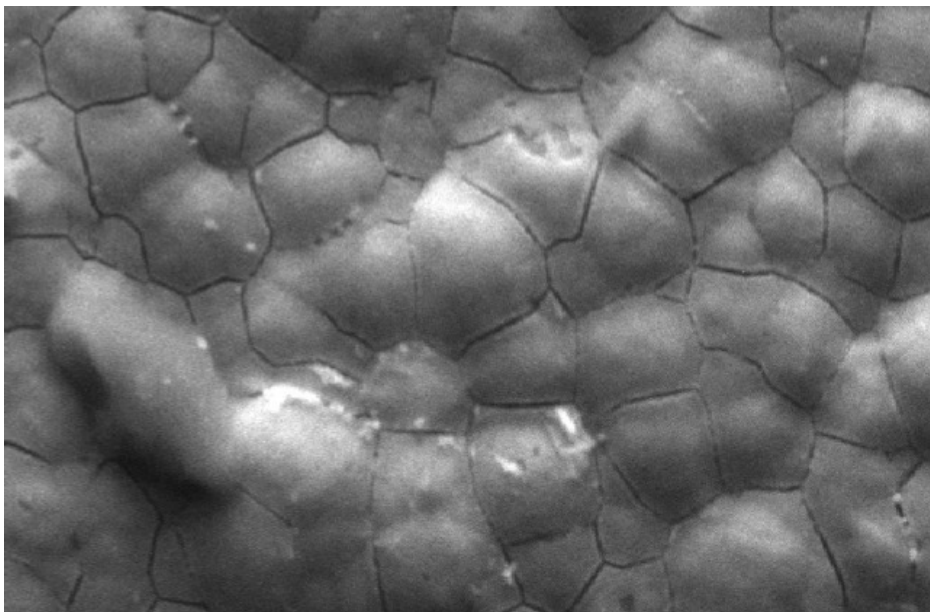
A key advantage of ENIG is that it offers excellent solderability and can retain this during prolonged storage prior to soldering assembly and during the multiple soldering operations encountered when assembling complex, high value electronics.

While it was predicted that ENIG's market share would increase significantly after implementation of the Restriction of certain Hazardous Substances Directive (RoHS) in 2006, the expected increase has not materialised due to a combination of cost, the emergence of some lead-free HASL alternatives and because of a fear of ENIG-specific problems which can lead to disastrous yields and product failures if they occur.

Another advantage of ENIG finishes is that they have excellent planarity and this is crucial when assembling and soldering small fine-pitched surface mount components. These are often of high value and placement accuracy is critical for achieving the required assembly yields. Unlike other coating technologies, which are applied solely to facilitate storage and solderability during soldering assembly, ENIG is a functional coating that utilises the solid-state properties of the nickel to stabilise the soldered interface, in effect, acting as a barrier layer to prevent the growth of tin-copper intermetallic compounds, which can embrittle the soldered joints during the service-life of the product.

This greatly enhances the reliability of ENIG-coated PCB assemblies, especially during prolonged use at elevated temperatures.

However, while ENIG coatings have a good reputation for excellent solderability, there are a number of technical and economic factors that can cause problems for PCB fabricators and their customers. The most widely recognised of these is referred to as 'black pad' which is thought to be attributable to excessive corrosion of the nickel coating during the subsequent immersion gold deposition process. Despite having been identified more than 10 years ago, the mechanisms that cause the effect (and the contributing factors) are still poorly understood.



A soldered ENIG pad after removal of the solder showing no intermetallic compound growth and the "mud cracked" appearance of the underlying nickel often linked to "black pad" (Courtesy ITRI Ltd)

Other problematic failure mechanisms include insufficient gold coating thickness, gold coating porosity, nickel migration, excessive phosphorus levels in the nickel layer, poor plating quality, excessive coating stress in the nickel, and general solderability degradation.

When ENIG-related problems occur they usually affect an entire product design or batch and the problems are often only identified after assembly, during which expensive components have been soldered to the PCBs.

Many ENIG-related problems are only identified later via field-failures and when this occurs, large sums of money are spent identifying and resolving the problem, usually by several members of the electronics supply chain.

In some circumstances, especially if liabilities and compensation claims are pursued, the total cost of an ENIG-related problem could be orders of magnitude higher than the cost of the PCBs supplied by the fabricator. It is probable that any ENIG user who has been using the finish for a substantial length of time will have experienced some of these problems.

One of the ASPIS project partners, ITRI, has extensive experience in diagnosing and troubleshooting ENIG-related problems. Such problems are highly sensitive commercially and are virtually never revealed publicly due to the potential financial ramifications and loss of reputation.

In one investigation ITRI conducted a particular design of mobile phone was experiencing failure rates in excess of 50% in post-assembly drop tests. Three PCB suppliers' boards had been used for the product, of which two suffered high levels of failures. Laboratory testing showed that one of the suppliers' boards was experiencing a 'black pad' corrosion issue, whereas the other's board was affected by excessive gold coating porosity which had led to oxidation of the underlying nickel and poor solderability.

Another 'black pad' problems occurred with two different avionics systems in a single year. One was an engine controller board and the other an auxiliary system board. Both problems required immediate servicing to replace potentially affected boards from aircraft and replacement stocks. Emergency manufacturing of replacements had to take place. As well as the direct costs of replacement and troubleshooting the problem, significant disruption was caused to flight operations, seriously impacting the end-users' day-to-day operations. Discussions with large European electronics manufacturers have confirmed their concerns about nickel-gold finishes.

The ASPIS project aims to help both the European PCB fabrication and broader electronics industries by developing new chemical processes, as well as methods for predicting, avoiding and detecting ENIG related issues. Currently, the failure mechanisms are not fully understood and, therefore, the factors which could contribute to them are not all known. This prevents fabricators and assemblers from properly optimising their processes and users from predicting or even identifying which PCBs might be affected or by which type of mode products have failed.

The ASPIS project also aims to strengthen the European electronics industry supply chain, from material suppliers to end producers, by helping ENIG users and by offering enhanced coating technologies with similar solderability and reliability benefits.

It is important to support ENIG users because PCB fabricators' customers will continue to specify it for their products, regardless of whether new alternatives emerge. This will be due to familiarity, the lack of historical data of field reliability and because purchase specifications exist which cannot be changed without requalification; a long and expensive process.

For these people, the fundamental knowledge developed in ASPIS will help them to identify and avoid design and process-related factors which can increase the risk of failures occurring. As ENIG will continue to be used on existing boards, which obviously cannot retroactively be subject to these precautions, the knowledge gained will also enable engineers to identify key areas to investigate

in order to validate the quality of the ENIG coated boards.

The ASPIS project will also reduce the likelihood of ENIG-related problems occurring by improving the coating deposition technologies. Unlike current developments, which have largely been undertaken empirically, the fundamental knowledge developed will be used to intelligently target specific improvements.

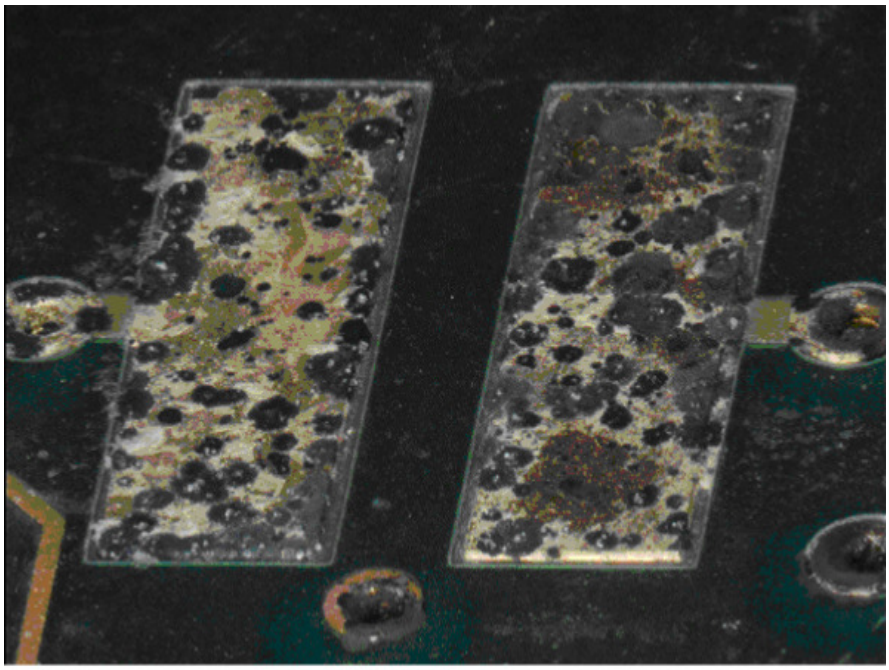
For example, one important area to be addressed will be the thickness of the gold deposited. Sufficient gold is required to provide a continuous non-porous film but, as this thickness increases, so does the cost and there can also be a negative impact on solder joint reliability.

Through specific work packages focussing on plating development the ASPIS project aims to develop new or enhanced processes that will enable thinner coatings to be used, thus reducing the cost of using ENIG while offering longer term reliability enhancements.

Another key goal is to develop methods for identifying potential problems related to the use of ENIG on PCBs and two key approaches will be investigated. The first will be to develop laboratory methods for identifying which failure mechanism caused a particular problem. The second method is to develop a non-destructive screening method that can be used at the PCB fabricator or electronics assembler in order to identify problems on boards before components are soldered onto them.

Therefore, another key aim of the ASPIS project is to build a prototype instrument for demonstration and validation purposes.

One way to prevent ENIG-related problems is to avoid them altogether by using different coating technologies, either via different deposition methods or by the use of alternative materials or structures.



ENIG coated pads after acid vapour exposure revealing the presence of pores in the coating (Courtesy of ITRI Ltd)

Specific work packages of the ASPIS project will investigate and develop alternative deposition methods from aqueous solution and ionic liquids respectively.

Most, though not all, of the methods for depositing different metals from aqueous solution are well established and are used for other applications. The novelty is applying them to this high reliability, functional, solderable coating technology.

Plating from ionic liquids is a more recent development and is not yet used in the PCB fabrication industry. However, it is known that metal films deposited from ionic liquids can exhibit improved properties which may, for example, enable thinner coatings of gold to be used or even alternative barrier layers to be deposited.

The current lack of in-depth understanding of the nickel-gold process means that no design rules exist for avoiding problems such as 'black pad', nor are there standards in place that can be used to minimise the risks.

The most widely applied industry standard, the IPC 6010 series, merely specifies a minimum coating thickness for the nickel and gold layers of 3.00 μm and 0.05 μm respectively for coatings on rigid boards.

The knowledge, data and experiences gained and accumulated in ASPIS will be used to improve and expand the industry standards and purchasing specification requirements.

Improved ENIG or alternative coating technologies will, likewise, require applicable standards in order to get industry acceptance.

The new information and methodologies being developed by the ASPIS project will help reduce the number of ENIG-related problems reaching production and also accelerate investigations and appropriate response times. This will reduce associated costs and increase customer confidence in the ENIG process.

The development of an assembly line tool for identifying problematic PCBs will reduce lost production costs and lower the risk of field-failures and their potential consequences.

The development of improved and alternative coatings technologies will also enable European PCB fabricators and their customers to produce more

competitive products via both increased process and assembly yields at subsequent higher levels of quality in finished products. Reducing the quantities of nickel and gold used in the solderable coatings by improvement or replacement will also reduce the overall cost of the PCB finish and also help the European electronics industry to adopt more sustainable approaches to materials use.

Further information on the ASPIS project will soon be available from a dedicated website and there will also be a wide range of dissemination activities throughout the life of the project. These will include ongoing updates in this journal. In the meantime, further information can be obtained directly from the project co-ordinator at

martingoosey@aol.com.

Martin Goosey

ASPIS Project Coordinator

January 2011

Abbreviation	Full Name
ASPIS	Advanced Surface Protection for Improved Reliability PCB Systems
EIPC	European Institute of Printed Circuits
ENIG	Electroless Nickel - Immersion Gold
HASL	Hot Air Solder Level or Leveling
ICT	Institute of Circuit Technology
IPC 6010	IPC's current qualification and performance specification standards for all major types of printed boards.
ITRI Ltd	Name of Company
RoHS	Restriction of the use of certain Hazardous Substances Directive
TNO	Nederlandse Organisatie voor Toegepast Natuurwetenschappelijk Onderzoek (Netherlands Organization for Applied Scientific Research).

The Institute of Circuit Technology
Winsford Evening Seminar

February 1, 2011

Winsford in Cheshire, towards the north-west of England, proved a popular new venue for The Institute of Circuit Technology's series of evening technical seminars. The inaugural Winsford event, kindly sponsored by **C C Electronics Europe**, brought together a fifty-strong group of PCB professionals including that stalwart of the industry Dennis Price, returned to health after serious illness, to the delight of all present.

Before introducing the seminar programme, which included papers on applications of ultrasonics, embedded RFID, automatic panel handling and via filling, ICT Chairman **Professor Martin Goosey** described the participation of ICT in a new European research project to develop novel new and improved nickel-gold solderable finishes. The three year project is known as ASPIS, an abbreviation of Advanced Surface Protection for Improved Reliability PCB Systems, was being supported via the European Commission's 7th Framework programme, with twelve partners from across Europe, including four key research organisations.

The ASPIS project aimed to help the European PCB fabrication and broader electronics industries by developing new chemical processes and methods for predicting, avoiding and detecting ENIG related issues.

ICT were undertaking the dissemination activities to bring the technology to the attention of the European PCB and assembly industries.

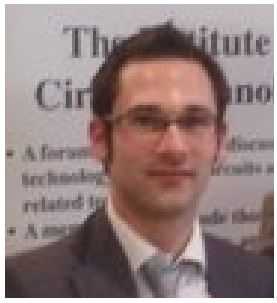
See also Pages 3-6 for more information.

The first seminar speaker, **Dr Andy Cobley,** Head of Materials at Coventry University's Sonochemistry Centre, reported the progress of a study of the use of ultrasound to enable the permanganate desmear process, which traditionally involves high temperatures, long process times and hazardous chemistry, to be successfully carried out at lower temperatures and concentrations.

Initially supported by the Innovative Electronics Manufacturing Research Centre, work had continued with funding from the Technology Strategy Board. Dr Cobley explained the principles of ultrasonic cavitation and the phenomenon of microjetting, which on a microscopic scale could produce extreme temperature and pressure effects at surfaces, capable of breaking chemical bonds and generating free radicals which, together with a mechanical scrubbing and cleaning action, could result in significant surface modification of materials. Moreover, ultrasonics could destroy boundary layers and facilitate the movement of reactants and byproducts to and away from the surface. Initial work using water alone had demonstrated and quantified the principal parameters: frequency, intensity and temperature, and provided a technology platform as a baseline for further development and eventual commercialisation.

Recent work, directed at the desmearing of drilled multilayer test pieces, had examined the effect of ultrasound at various temperatures and permanganate concentrations, and had indicated that smear removal was generally better with ultrasound and that using ultrasound it had been possible to produce samples free from interconnection defects with full strength and half strength permanganate at 60 ºC.

Funding was currently being sought to enable further process validation, to scale up from laboratory to process demonstrator and to explore the applicability of sonochemical principles to other process areas.



Axel Bindel, a Research Associate at Loughborough University, was working on a collaborative research project involving PCB fabricators and assemblers, avionics and automotive OEMs, and recyclers, directed at the development of a product and process monitoring system for electronic assemblies using embedded radio frequency identification (RFID).

The objective was to reduce the lifecycle costs of manufactured products by embedding intelligent information which would increase the observability and traceability of the product through the whole electronic manufacturing supply chain: PCB fabrication and assembly, original equipment manufacturing and recycling.

The project partners were examining techniques for embedding RFID devices within the PCB, and developing software for selecting and handling the product information stored on them.

Bindel gave an overview of the principles of RFID and its advantages over optical systems such as bar codes, particularly that no line-of-sight was required, then described the additional processes required at the lay-up and bonding stages of multilayer

circuit board manufacture. The physical dimensions of an RFID chip were relatively small, typically about 450 microns in X and Y, but additional area was required within the circuit pattern to accommodate the antenna. No internal power supply was required: the chip was energised by electromagnetic induction from the reader.

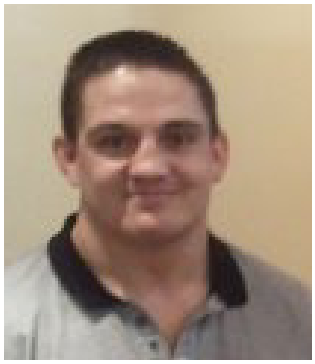
Manufacturing considerations included the number of plies of prepreg to use, the size and shape of the recess required, and the temperature and pressure of the bonding process. Interconnection could be achieved using conductive adhesives or solder paste. Although early trials had given poor yields, with problems of chips breaking, yields were continuing to improve and were now better than 70-80%, with chips maintaining their functionality through the thermal shocks of hot-air solder leveling and reflow. Good progress had been made with software development and applications were being evaluated in electronics manufacturing and recycling.

Potential end-users had shown great interest, particularly in the automotive industry.

Leon Benmayor, from **Gabriel Benmayor SA** in Spain explained the benefits of automatic panel handling in PCB processing: reduced labour costs, reduced scrap and increased productivity, and went on to describe a range of proprietary equipment which included loader-unloaders, conveyors, angle diverters, turning and rotating devices.

He used video to illustrate their principles of operation and special features designed to maintain direction, sense of flow and spacing between panels, to handle thin and flexible material, and safety devices to avoid damage to the work in case of malfunction.

Particularly fascinating to watch in action was a loader specially developed to automate the workflow through a laser direct imaging machine. To achieve the complex motion required, the loader was equipped with a six-axis robot arm, together with a double manipulator to reduce cycle time. It could handle panels from 50 microns to 3.2 mm thick, carrying them from an input cassette, aligning them on the LDI machine then removing them to an output cassette after exposure. An additional benefit was that the machine could be programmed either for normal series operation or, if a first-off or prototype batch was required to be fast-tracked through the system, to feed layers sequentially to expose for example sides 2 and 3, 4 and 5, 6 and 7 in succession.



Final presentation came from **Martin Bunce** of **MacDermid**, who posed the question "Why fill via holes?" then went on to explain the reliability benefits of filling blind microvias with electrodeposited copper.

Many PCB designs included blind microvias and plated through-holes on the same panel, creating a market demand for an electroplating process that would fill vias and plate through-holes simultaneously. MacDermid had responded by developing a proprietary acid copper chemistry with deposit properties meeting IPC specifications for tensile strength elongation and solder shock, whilst offering a through-hole distribution of 87% on 4:1 aspect ratio.

Bunce explained the mechanism of via filling. The process flow was standard except for a predip prior to the copper bath designed to enhance bottom-up plating. The predip uniformly coated the panel with an accelerator, which was removed from outer surfaces by mild rinsing, but not from the bottom of the microvias. The plating bath itself contained a suppressor, which was absorbed on to the outer surface but was prevented by the accelerator from absorbing on the base of the microvias. The accelerator promoted the selective deposition of copper and as the via began to fill, deposition speed was enhanced as the curvature within the hole decreased. As the plating in the via approached the outer surface, a leveller displaced the accelerator and inhibited further plating, leaving a near-planar surface.

Microvia geometry influenced filling efficiency: undercut profiles and exposed glass fibres could present difficulties, and quality of primary metallisation was critical. Extensive qualification tests had been carried out both by MacDermid and their customers, and physical properties had exceeded customer expectations.

No extraordinary equipment set-up was needed to operate the process and it had a wide capability range, whether in panel plate or pattern plate format.

Professor Goosey brought the seminar to a close and thanked all who had attended, and particularly CC Electronics Europe for their support.

He commented that the membership of the Institute continued to grow at an encouraging rate and that regional seminars clearly provided good opportunities for circuit

technologists to get together, learn about new developments, network and share opinions and experiences with their counterparts in the industry.

Pete Starkey

ICT Council

6th February 2011

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Winsford Evening Seminar 1st February 2011

The Institute of Circuit Technology
Arundel Evening Seminar

1st March 2011

Bill Wilkie, ICT Technical Director, welcomed over 50 delegates to an evening meeting at the Norfolk Arms Hotel, Arundel.

Bill reminded the delegates that the ICT is in its 37th year since it was founded. For the first time ever the ICT is holding an annual symposium which is free to members and will include a sit down lunch. The symposium is scheduled for 1st June at the Coventry Technocentre.

The Annual Foundation Course in PCB Technology is being held from 11th to 15thApril at Loughborough University with 20 delegates registered so far.

This is a valuable opportunity for newcomers to our industry to gain a comprehensive knowledge of PCB manufacturing processes. The ICT web site has full details of this and future events.

www.instct.org.

Bill also advised of the key role ICT has a in the administration and dissemination of a European research project – ASPIS. The aim of the project is to develop a more reliable Electroless Nickel - Immersion Gold surface finish. The web site has been launched and can be viewed here.

www.aspis-pcb.org

Also see pages 3-6.

The first speaker for the evening session was

Tom Brown of Holders Technology. His paper was titled "**FR4ever**".

Tom explained we are an industry with process maturity. However, market forces are pushing the limits of accepted FR4 materials. There is an ever increasing demand for improved functionality from PCB's.

Tom highlighted 2 examples. 75% of mobiles sold in Europe are now smart phones with highly complex PCB's.

The production of high brightness LED's for solid state lighting is expanding rapidly. The application of solid state lighting produces significant thermal management challenges with heat output rising 10 fold from the accepted 4watts/sqin to 40watts/sqin.

Tom reviewed the new aluminium clad substrates that have been developed with enhanced thermal conductivity. While there will continue to be many applications suitable for FR4 it is definitely not

FR4 everything!

2. Our second speaker was **Dr Ron Kirby of Arlon.** His paper was titled "**High Frequency Materials for RF Applications in Base Stations**".

The introduction of 4G mobile phone technology is driving changes to base stations to cope with the higher data rates. We typically will see a downlink of 10-100 Mbps and uplink of 5-50 Mbps.

There are predicted to be in excess of 7 million base stations in Europe by 2014.

Cost is an important factor and commercial grades of RF substrates and PTFE for antennas are available. High performance RF materials are utilised in space and defence applications.

Thermally conductive materials are a key factor. Typically a 10ºC rise in temperature reduces mean time between failures by 50%.

Ron reviewed examples of ceramic filled low loss halogen free thermosetting laminates which have 2x - 4x greater thermal conductivity and high copper peel strength at an affordable cost.

3. The next paper, "**Advances in Mechanical Micro-drilling**" was presented by **Chris Gerrard of Westwind.**

Chris reviewed the background of the PCB drilling market, the recent history of global manufacturing and the current worldwide distribution of production and sales. Also the current technology of spindles and machines, and an overview of the developments in spindle technology.

Manufacturing of spindles is divided between UK and China. Mechanical drilling of 75µ holes is now available and 50µ drill bits will be available in 2016.

Calculation of the peripheral cutting speed shows that spindle speeds in excess of 900,000 rpm will be required to achieve optimum drilling conditions!

Optimum spindle speeds give longer tool life, less tool breakage, improved hole quality and higher productivity.

The next generation of drilling machines will achieve 850 to 1000 hits per minute. They will need to be highly rigid and thermally stable.

China is lagging behind Japan and Europe in producing machines capable of micro-drilling. There have been a number of established European and American drilling machine manufacturers who have closed as a result of not reacting to the market changes driven by China and Asia.

Air bearing spindles can achieve very high rotational speeds. The next phase of spindle development will achieve 370 k rpm using 2 mm collets by 2012.

Laser drilling is expected to dominate in the sub 50µ applications but mechanical

drilling is a strong competitor in the 50µ to 100µ range.

4. "**Making the Most of UL PCB Recognition**" was the title of our final paper from **Emma Hudson of Underwriters Laboratory.**

Emma gave a comprehensive review of the PCB categories that are recognised and the procedures for achieving product recognition for manufacturing facilities.

Costs can be kept to a minimum by careful planning of process and temperature requirements.

Reduced or no-test programmes are available for adding materials through the CCIL (copper clad industrial laminate) program.

Emma demonstrated how the ULIQ searchable database can be used to optimise the recognition parameters for a PCB manufacturer.

Similar cost savings can be achieved by using the Permanent Coatings Program for solder mask selection. UL listing cards can also be searched to match facility recognition with customer requirements.

Bill Wilkie concluded the evening by thanking Gillian Herriot, Managing Director of Holders Technology, for sponsoring the event.

Richard Wood-Roe
ICT Council
5th March 2011

The Institutes Web Site has links to .pdf files of the original presentations.
www.instct.org.
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The Presenters of the Technical Papers at Arundel 01/

Chris Gerrard, Emma Hudson, Ron Kirby
Gillian Herriot, Tom Brown,

Plastic Electronics: the challenges for low temperature manufacturing

The Hauser Forum, Cambridge

15th March 2011

The Innovative Electronics Manufacturing Research Centre (IeMRC) and the Cambridge Integrated Knowledge Centre (CIKC) held a one day plastic electronics seminar on the 15th March at the Hauser Forum in Cambridge. The seminar had a specific focus on the challenges and opportunities for new low temperature manufacturing techniques in photonics and electronics and the clear level of interest in the subject was confirmed by the 123 people that attended the event. The full programme included ten speakers from both industry and academia, who covered a wide range of important subject matter relating to plastic and printed electronics.

The seminar began with a welcome from **Dr Chris Rider, Director** of the **CIKC**, who also introduced the first speaker **Dr Steve Jones**, of **Printed Electronics Ltd (PEL).** Steve gave a presentation titled **'Printed electronics: where from here?'**

Electronics was about the interconnection and integration of components to form functional devices and it was now becoming widespread, ubiquitous and invisible. He also defined what constituted printed electronics and stated that it must enhance functionality.

Steve emphasised how producers in the Far East were now dominant in producing most of the world's electronics. . Taiwan's Foxconn, for example, was one of the biggest producers and was intending to increase its workforce to 1.3 million people over the next 12 months. The big question was how could other companies compete with these large organisations, especially in Europe, where the supply chains barely existed any more.

Printed electronics was still immature i.e. it was still largely at the demonstrator/proof of concept stage. Therefore, there was a need to find niche, new products moving into areas where electronics had not gone before e.g. for smart packaging and in anti-counterfeiting applications. Printed electronics had been over-hyped in the past, but there were fundamental gaps in the toolbox and the levels of integration that had been achieved were still considered to be poor.

Steve re-emphasised the huge potential that was available for printed electronics and gave examples of products that **PEL** had produced, including displays and logic devices.

Professor Henning Sirringhaus of the **University of Cambridge** then gave a presentation entitled **'Organic transistors for applications in flexible electronics'.**

Henning stated that the performance achievable with printed organic transistors (TFTs) was currently often inferior to traditional silicon devices.

Organic semiconductors had low mobilities, although substantial improvements had been made since the 1980s. He described the new organic materials that had been at the heart of this improvement and the enhancements achieved by downscaling.

New technologies and equipment were needed for defining the requisite smaller channel lengths. A new technique known as self-alignment printing was then detailed which enabled organic transistors to be made that could switch in the megahertz range. Complementary n and p type transistors could now be produced that gave approximately equal performances and work had been carried out to integrate these into logic type devices. Work had also been undertaken on metal oxide semiconductors, as these could provide another route to even higher mobilities.

In particular, the possibility of solution deposition had been investigated and this had required the development of appropriate alkoxide materials that could be spin coated onto amorphous substrates. This sol-gel route had been used to produce indium zinc oxide field effect transistors (FETs) that had then been characterised for performance and some of the data was shown e.g. mobilities of 8 to 10 cm/Vs had been recorded. Indium gallium zinc oxide thin film transistors (TFTs) had also been produced. Unlike the organic transistors, these metal oxide devices did, however, require some higher temperature processing stages.

Hazel Assender from the **University of Oxford** gave a presentation on the **'High speed vacuum deposition of organic TFTs in a roll to roll facility'**.

This IeMRC funded project was running at four universities, Oxford, Leeds, Manchester and Bangor and involved eight industrial partners. The roll to roll manufacturing capability of the project used the evaporation of an organic monomer to deposit a polymer on films such as PET to form transistor structures. It could run at five metres per second and handle films up to 350 mm wide. A larger and faster capability was also available via the industrial partner, Camvac.

The advantages and disadvantages of vacuum deposition were compared with solvent techniques. Vacuum was a low energy rapid process in which the deposition of multi-layers was relatively straightforward. The polymer

deposited was based on an acrylate chemistry and metals were also selectively deposited using an evaporation process.

Hazel then focused on the deposition of pentacene and described the impact of the deposition parameters on material performance.

The transistor's insulator layer was formed by the vacuum deposition of a monomer that was subsequently cured . Curing of the material had been studied using FTIR and by monitoring the dielectric constant of the polymerised film. The effect of insulator thickness on device performance and the shelf life of fabricated transistors had also been studied. The project had already demonstrated the ability to fabricate organic electronics in a roll to roll environment.

Dr Steve Thomas from **Conductive Inkjet Technologies Ltd (CIT)** then gave a presentation entitled **'Additive manufacture of interconnects'.**

Interconnects were traditionally based on the copper tracks of printed circuit boards but these needed multiple process stages, where labour and equipment intensive and wasteful of materials. An alternative was screen printing but this was also relatively expensive and used a lot of material.

CIT had focussed on a route that separated the printability from the conductivity by using an electroless copper plating approach and Steve described the chemistry of electroless deposition.

The concept was to ink jet deposit catalytic metals capable of initiating the deposition of copper. A key challenge had been to develop a suitable catalytic ink formulation and one such example also incorporated a UV curing system to give a very rapid transition to a cured film.

The reel to reel process enabled reduced processing costs via continuous processing and less labour input. An innovation in the equipment was the use of fluidics bearings.

Typical feature sizes produced were 220 microns and larger, with a printing speed of 20 metres/minute giving sheet resistances of 20 to 100 MΩ/square. Copper was deposited at a plating speed of 2 to 12 metres/minute and the metal was solderable using conventional surface mount technology.

The processing of finer features had also been developed using a photolithographic patterning process and this enabled features down to three microns to be produced.

Applications included making fine meshes for use with PEDOT to replace indium tin oxide.

The final morning paper was given by **Dr Andrew Flewitt** from the **University of Cambridge** and was on the selection of combinations of semiconductor/dielectric metal oxides deposited without substrate heating for transparent thin film transistors.

Andrew began by explaining why amorphous silicon continued to dominate in terms of large area electronic materials. This was because it was a known technology based on a stable non-toxic material that could be processed at low temperatures.

However, it also had low carrier mobility, incurred patterning costs and was metastable when in device operation.

A key alternative was metal oxide technology. Although this tended to be more of an unknown, it did offer amorphous microstructured materials via low temperature processing that could give high carrier mobilities. There was a range of materials that could be used and the oxides could also be used to form dielectric structures.

For a given application, the appropriate material technology had to be married with the optimum deposition and patterning processes.

Using metal oxides, it was possible to deposit transparent thin film transistors and these would find increasing use in sensor and touch screen applications.

Materials such as zinc tin oxide, cuprous oxide, indium zinc oxide, hafnium oxide and alumina had been deposited as pinhole free films that could be used in a range of devices.

A four mask process for producing thin film transistors was then described and the performance characteristics of a range of devices were presented.

The afternoon session was chaired by **Professor Martin Goosey, Industrial Director of the IeMRC** and, after reviewing the IeMRC's activities, he introduced **Richard Young from Brunel University,** who gave a presentation on **'Microcontact printing and applications'.** Richard described the work that at Brunel in recent years on offset lithography and printed electroluminecent displays. He then described the concept of soft lithography and microcontact printing, using a poly dimethyl siloxane (PDMS) elastomeric stamp. A single silicon wafer could be used for producing a range of individual PDMS stamps used in the microcontact process. The work to develop the thiol based inks used in the process was also described. A range of conductor track and gap sizes down to 25 microns had been produced for use in display structures, the stimulating voltages were reduced from 130 V to around 70 V in certain more electrically stable structures with 75 micron tracks and gaps. A range of frequencies had also been used to stimulate the phosphor particles. Richard had

looked at using the conductors in thermistor structures based on copper oxide. For the future, it was envisaged that sub-micron dimensions would be possible.

The next presentation was on **'Electronics via imprint'** and was by **Scott White of Pragmatic Printing Ltd**. The company had unique technology for making two dimensional semiconductors that was thus ideal for printing applications. Scott outlined the challenges for printed logic; one of these was being able to produce the smaller features required for increased performance and to reduce overall size. The Imprint processes used today had the capability to produce much smaller features at low cost and high volume. Features down to a few nanometres could now be made. The process was detailed and the first stages were similar to microcontact printing. There were then a range of process options, including direct embossing into functional materials, patterning of a resist for subsequent pattern transfer and pre-patterning of a substrate for selective deposition. An example of an imprint stamp was shown that exhibited nanometre-scale features. These approaches could then be used to produce novel devices with complex 3D structures and multiple material layers. The 3D imprint processes enabled self aligned structures to be formed. Simple 2D planar nanotransistors could also be produced with sub-micron features and a single semiconductor layer. An initial application in low cost non-invasive printed logic labels was cited. These required easy assembly on polyester, paper or card. Demand for electronic smart packaging devices had been valued at around $7.7 billion in 2010 and there was a growing need for new printed security devices. Scott concluded by summarising that imprint technology provided a unique platform for printed logic.

Dr Daping Chu of the **University of Cambridge** then gave a talk entitled **'Laminated electro-active foils – liquid crystal transflective panels'.** Dr Chu outlined the trends in display technology from 1980 out to 2040 and it was clear that there was going to be a very large growth in demand for reflective display types. He then described electro-optic bistability in smectic liquid crystals and its potential use in e-ink 'newsprint' displays. By using a black dyed cell, it was possible to achieve a reflective contrast of >7:1 with a very large number of pixels that could be multiplexed. Much work had been carried out to develop high stability dyes for these applications and, in particular, there was a need for coloured dyes that could be used in full colour displays. Dr Chu described the technical and commercial objectives of the 'LEAF' project that was addressing a number of specific aspects of display manufacturing. Its key objective was to develop technology for plastic envelope liquid crystal displays. This work included the characterisation of a wide range of materials. He then showed the facilities available within the Centre for Advanced Photonics and Electronics (CAPE) at Cambridge, before giving some examples of displays that had been made, including coloured plastic cells. These could be combined in stacks to provide full colour reflective displays and a possible process flow for making such displays was described. Work had also been undertaken to produce UV durable colourants and to replace indium tin oxide with graphene in transparent electrodes. Plastic electroactive foils would find large area applications in smart windows but, if full colour displays could be produced, there would be many more applications e.g. in large area advertising signage and for changing a building's décor. Other potential applications included transparent antennae and photovoltaics.

The penultimate presentation entitled **'Towards roll to roll production of organic photovoltaic modules'** was given by **Dr Keiran Reynolds of eight19 Ltd.** New designs and printing processes would revolutionise the way that photovoltaics were built and eight19 was developing the technology and manufacturing approaches needed to make plastic photovoltaics a reality. In 2009, 1.45 billion people lacked access to electricity and there was thus a huge opportunity for providing 'off-grid power'. One example was to develop a lighting unit that could provide 2 to 5 Watts for 5 hours per day. There could be a demand for up to 2 million of these in India alone by 2017. Organic photovoltaics had the potential to offer a number of real advantages over conventional approaches and these included solution processing, robustness and light weight. The power conversion efficiency of these devices was gradually increasing and was currently at ~8.3%. The structure of such an excitonic solar cell was described and shown to be different to that of a conventional solar cell. Kieran then discussed some of the deposition challenges eg for forming the semiconductor composite structures and the associated morphology control.

The final presentation of the seminar was given by **Professor Richard Penty of Cambridge University** and was on **'Polymer interconnects for datacom and sensing'.** As data rates and frequencies continued to increase, there was a growing need to use optical interconnects to augment traditional copper technology. However, the technology also needed low cost components that

were compatible with conventional PCB manufacturing processes. A siloxane based material from Dow Corning was available that exhibited suitable mechanical, thermal and optical properties for wave guide applications. Multimode waveguides had been deposited on FR4 substrates with cross sections of a few tens of microns. The fundamental transmission properties of these waveguides were described and it had been found that very low crosstalk could be achieved between adjacent waveguides. Also, waveguides crossing each other at ninety degrees were effectively lossless and cross talk was better than 30 dB. A polymer back plane application had been considered for utilising the optical waveguide approach and a 10 card optical design was described that had 100 waveguides in total. There was widespread industrial interest in the use of optical back planes and many of the larger electronics companies now had their own design concepts. The challenges of providing optical coupling schemes were described and the aim had been to produce a low complexity, low cost optoelectric PCBs. The design adopted was based on a low cost double sided FR4 board in which the electrical layout and vias were processed first. Waveguides were then fabricated on the bottom board surface and the components were attached using a solder reflow process. A through board L connector was then used to provide the optical interconnections. The optical performance of such an assembly was shown. The presentation concluded with a discussion of the use of sensitised waveguides that could act as gas sensors. Work had also been carried out to develop a screen printing method for polymer waveguides.

The seminar had covered a wide range of plastic and printed electronics applications including, interconnects, semiconductors, sensors, photovoltaics, optical waveguides and displays. There had been a strong focus from all of the presenters on addressing the manufacturing challenges and on taking their work towards real commercial applications. In summary, this was an excellent seminar that attracted a large audience from both industry and academia.

Martin Goosey

15th March 2011

Group Members of The Institute of Circuit Technology April 2011

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The Membership Secretary's notes - April 2011

The first quarter of the year is always a busy time for the ICT, with evening seminars in the Northern and Southern areas and our Annual Foundation Course in PCB Design and Manufacture at Loughborough University. This year has been no exception, with well attended seminars at Winsford and Arundel and a registration class of 15 for the Foundation Course. At the same time, we are also preparing for our Annual Symposium at the Coventry Technocentre, which, in a first for the ICT, is free to Members. We have had a good response to our call for papers and are busy preparing the Agenda.

Membership Numbers are still around the 230 mark, with a steady trickle of applications, balanced by the inevitable background of members leaving the Industry or retiring.

During this period, we have also been busy cooperating with other like parties, such as the EIPC, where we have traded our Journal for their SpeedNews on our website. We have also contributed to the IMF website to increase hits and are always pleased to see our events displayed on the Electronic Yorkshire - ey. Bulletin.

We share information with SMART group and also Livingston based MNI, the trade association representing the UK Semiconductor, Microelectronics and Electronic Systems Communities – so as you can see, we are not alone!

Bill Wilkie

Institute of Circuit Technology
Northern UK Circuit Group

2011 Annual Foundation Course
in
PCB Design and Manufacturing at Loughborough University
Monday 11th April – Thursday 14th April

DAY 1 at Tamworth

- Monday 11th April

9.30-10.00 **Enrolment at Invotec Tamworth /Coffee**

10.00-11.15 **Basic Manufacturing Sequence**
Mr Steve Kerr - Invotec Group

11.15-12.30 **Design for Manufacture**
Mr Mike Osmond-Intrasys Design

LUNCH

13.30- 14.00 **Digital Manufacturing Plant Tour**
Mr Neil Chilton - Printed Electronics

14.00- 15.00 **Plant Visit - Invotec - Tamworth**

DAY 2 at Loughborough

- Tuesday 12th April

900- 10.00 **Manufacture of PCB & M/L Laminates**
Mr Geoff Layhe - Lamar Group

10.00- 11.00 **Programming, Drilling & Routing**
Mr Gavin Barclay - ACS Ltd

11.00- 12.00 **Photographic Processes**
Mr John Dingley - Agfa PCB Products

LUNCH

13.00- 14.00 **Etching & Pre-Treatment Processes**
Mr Tom Parker - CCE Europe

14.00- 15.00 **Photomechanical Processes**
Mr John Rankine - Eternal Technology Corporation

15.00- 16.00 **Through Hole Plating & Multi-Layer Desmear**
Mr Steve Hirst - Chestech Ltd.

DAY 3 at Loughborough

- Wednesday 13th April

9.00- 10.00 **Soldermask Application Processes**
Mr Grant Bradley - Electra Polymers Ltd.

10.00-11.00 **Surface Preparation and Adhesion Promoters**
Mr Nigel White - Atotech Ltd.

11.00-12.00 **Alternative Surface Finishes**
Mr Nigel White - Atotech Ltd.

LUNCH

13.00-14.00 **Environmental Considerations**
Professor Martin Goosey - Loughborough University

14.00-15.00 **Assembly, Fusing & Soldering**
Professor Martin Goosey - Loughborough University

15.00-16.00 **Principles of Plating Copper & Tin Lead**
Dr Andy Cobley -Coventry University

DAY 4 at Loughborough

- Thursday 14th April

9.00-10.00 **Automatic Optical Inspection**
Mr Andrew Norton-Peplertech

10.00-11.00 **IECQ using IPC Standards**
Mr Dennis Price - Merlin Circuit Technology

11.00-12.00 **Embedded Devices**
Mr Dennis Price - Merlin Circuit Technology

LUNCH

12.30-13.30 **Digital Manufacture**
Dr Steve Jones - Printed Electronics

13.30 **Course Review**

For all information :- bill.wilkie@InstCT.org