Journal of the Institute of Circuit Technology

Contents

Vol.5 no.3 July 2012

2012 Events

12th June *Tuesday*
38th ICT Annual Symposium
at **Imperial War Museum, Duxford**
bill.wilkie@InstCT.org

29th June *Friday*
Dissemination Seminar
Results from Applied Research Projects in the Surface Engineering and Printed Circuit Sectors by the Surface Engineering Association
at Federation House, 10 Vyse St., Birmingham
info@sea.org.uk

4th September *Tuesday*
17.00 Registration
17.30 ICT Evening Seminar.
'UK PCB Manufacturing in association with the rest of the world'
bill.wilkie@InstCT.org
Newtown House Hotel, Hayling Island
http://www.newtownhouse.co.uk/
supported by Spirit Circuits.

6th September *Thursday*
20th Southern **PCB Golf Day** at the "The Wiltshire Golf and Country Club".
rwoodroe@aol.com

Editorial

Bill Wilkie
Membership Sec. & Director

Dr Andy Cobley
Deputy Chairman

John Walker
Hon. Secretary

Annual General Meeting held after the 38th Annual Symposium at the Imperial War Museum, Duxford on Tuesday 12th June 2012

This formal meeting, when the Council Members were supported by 20 - 30 Members, proceeded at the usual pace for such an occasion, several motions were proposed and voted, and then when we came to " Any other business " a Member raised a question of very great interest to me – "could the *Journal* be published in hard copy form"

At regular intervals this matter has been raised at Council Meetings together with the question about how many read it anyway. It was heartening to learn how many Members at the AGM would like to receive hard copies.

The subject is being investigated and costed.

Bruce Routledge

Copies of the Minutes from bcsbasingstoke@btinternet.com

Council Members 2011/2 Martin Goosey (*Chairman*), Andy Cobley (*Deputy Chairman*), John Walker (*Secretary*), Chris Wall (*Treasurer*), William Wilkie (*Membership Secretary & Events*), Bruce Routledge (*the Journal*), Richard Wood-Roe (*Web Site*), Lawson Lightfoot, Tom Parker, Steve Payne, Peter Starkey, Francesca Stern, Bob Willis.

Membership

New members notified by the Membership Secretary

10235	Alan Stevenson A.Inst.C.T.	10250	Aftab Thakur A.Inst.C.T.
10236	Barbara Waugh A.Inst.C.T.	10251	Stephen Bamsey A.Inst.C.T.
10237	Scott Thomson A.Inst.C.T.	10252	Stephen Cordy A.Inst.C.T.
10238	William Poskitt A.Inst.C.T.	10253	Alex West A.Inst.C.T.
10239	John Jacquest A.Inst.C.T.	10255	Matt Norris A.Inst.C.T.
10240	Paul Munday A.Inst.C.T.	10256	Lilia Quattrin A.Inst.C.T.
10241	Jolene Kitcheman A.Inst.C.T.	10257	Ian MacPhee A.Inst.C.T.
10242	Darren Borg A.Inst.C.T.	10258	James Warrener A.Inst.C.T.
10243	Stuart Gardiner A.Inst.C.T.	10259	Sandy Sydenham A.Inst.C.T.
10244	Pete Smith A.Inst.C.T.	10260	Louise Bailey A.Inst.C.T.
10245	Nigel Brindley A.Inst.C.T.	10261	Harry Payne A.Inst.C.T.
10246	Andrew Gorse A.Inst.C.T.	10262	Will Crew A.Inst.C.T.
10247	Andy Ewings A.Inst.C.T.	10263	Roy Garside A.Inst.C.T.
10248	Scott Stephenson A.Inst.C.T.	10264	Mark Margiotta M.Inst.C.T.
10249	Chandni Sudera A.Inst.C.T.		

Corrections and Clarifications

It is the policy of the Journal to correct errors in its next issue.

Please send corrections to : -

bruce.rout@btinternet.com

The Journal of the Institute of Circuit Technology is edited by Bruce Routledge on behalf of the ***Institute of Circuit Technology.***

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PCBs in the year 2020 —

What can the

IPC 2011 Technology Roadmap

tell us ?

by Len Pillinger

PCBs in the year 2020 —

What can the IPC 2011 Technology Roadmap tell us?

I have to admit that I have had little to do with printed boards on a day-to-day basis over the last five years since leaving BSI Product Services. Even while I was still at the BSI I relinquished responsibility for PCB industry certifications several times to concentrate on managing the team, but the PCB responsibility kept bouncing back. As my current employer's 'Product Compliance Manager' I am now regrettably more concerned with the end product rather than individual components.

Late last year a colleague asked for input to a Technology Roadmap for our future PCB requirements. Naturally I was only too willing to help. The next question was where to find some data of sufficient provenance to calibrate in-house capability against. I was aware that IPC published a biennial Technology Roadmap and managed to find some limited 2009 data on the internet (without having to buy a copy!). The roadmaps detail current data and predicted trends based on having polled the opinions of the 3200+ IPC worldwide membership.

Once I had managed to get hold of a copy of the 2011 Roadmap, I was immediately impressed. I had expected reams of dry statistics and little else. The roadmap actually consists of six parts:

Part A: a 'How to use guide'
Part B: Technology Trends
Part C: Design Considerations
Part D: Interconnections and Substrates
Part E: Assembly Technology
Part F: An appendix with some useful Standards and explanations of Terms and Acronyms.

The information that I found of most interest was in A3 'Emulator Details' which needs a sexier title to highlight the useful information it includes. This fifty-seven page analysis follows a format that respects the electronics supply chain. PCB capability does not erupt spontaneously; it is driven by the expectations of those organisations higher-up in the food chain. I have yet to delve into the bulk of the Roadmap and so this 'informal review' only really applies to A3.

Consumers demand electronics that is faster, lighter, more reliable, cheaper, less power hungry and greener. Designers take this into account and drive component manufacturers to create components to achieve these aspirations. This often means more I/ Os and a finer pitch. PCB assemblers expect the PCB fabricator to be ready to satisfy this need. It also follows that suppliers to PCB fabricators have to be ready with new materials, chemistry or processes. It is easy to see why a roadmap is worthwhile.

Unlike the creatures in George Orwell's Animal Farm, not all PCBs are created equal. The IPC Technology Roadmap addresses this with a series of 'emulators' which are intended to approximate to the range of board types and customers that make up the broad spectrum of the electronics industry. Consumer products are often the driver of new technology but reliability is not necessarily paramount. The military and avionics environment demands a more tried and tested approach.

A3 details a series of predictions based on the members' inputs on an emulator-by-emulator basis. The tables that follow have been selected on a pick-and-mix basis so as to give a taster of what is included rather than full detail of any given emulator. You need to buy your own copy for that!

Compared with the limited 2009 IPC Roadmap information that I have access to, their members are much less bullish about future technology trends. Research and Development budgets have presumably suffered as a result of the global recession.

Table 1 - Design Influences

PCB TECHNOLOGY FACTORS			Current 2010-2011		New Term 2012-2013		Mid Term 2014-2016		Long Term 2016-2020	
TECHNICAL DRIVER	METRIC	EMULATOR	RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
On-chip time rise	ps	Telecoms Module	1000	800	1000	800	900	500	800	450
On- chip frequency	GHz	Consumer Interposer	0.7	0.9	0.7	1	0.8	1	1	12
Minimum Device Voltage	Vdc	Telecoms Interposer	1	0.8	0.8	0.6	0.8	0.4	0.5	0.4
No. of Voltage Levels	No.	Automotive	3	4	3	4	2	3	2	3
Maximum Voltage	Vdc	Consumer Portable	120	200	120	200	140	200	160	220
Chip- to- PCB Speed	Gbits/sec	Telecoms Product	1400	3200	1800	3800	4000	4800	4000	5600
Thermal Dissipation	W(Max)	Automotive	25	40	30	45	40	60	40	60
EMC Susceptibility	Yes/No	Various	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Life Expectancy	Hours MTTF	Automotive	18000	26000	20000	28000	22000	30000	24000	36000
Operating range	T℃ min	Automotive	-10	-10	-10	-10	-10	-10	-10	-10
	T℃ max		45	55	45	55	45	55	45	55
PCB Temperature	T℃	Automotive	60	70	65	80	65	80	70	90
SOME LIMITED COMPARISON WITH PREVIOUS IPC TECHNOLOGY ROADMAPS										
	2011				2009					
On-chip time rise	Reduce 20% over 6 to 10 years				Reduce 60% over 6 to 10 years					
On- chip frequency	Increase 43% over 6 to10 years				More than double over 8 to 10 years					
Minimum Device Voltage	Halve over 6 to10 years				Halve over 6 to10 years					
No. of Voltage Levels	From 3 to 2 over 6 to 10 years				From 3 to 2 over 6 to 10 years					
Maximum Voltage	Increase 33% over 6 to10 years				Increase 75% over 8 to 10 years					
Chip- to- PCB Speed	Increase 186% over 6 to10 years				Increase 280% over 8 to 10 years					
Thermal Dissipation	Increase 60% over 6 to10 years				Increase 100% over 8 to 10 years					

Table 2 - Assembly Influences

PCB TECHNOLOGY FACTORS			Current 2010-2011		New Term 2012-2013		Mid Term 2014-2016		Long Term 2016-2020	
TECHNICAL DRIVER	METRIC	EMULATOR	RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Leads/Component	Average	Tablet computer	12	14	12	14	14	16	14	16
Max.No. of leads/component	Max I/O count	Telecoms Product	20	280	260	310	340	460	420	600
I/O pitch array packages	Min. mm	Tablet computer	0.5	0.4	0.5	0.4	0.4	0.3	0.3	0.25
I/O pitch peripheral array Packages	Min. mm	Various	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.4
I/O Chip scale or flip-chip Packages	Min. mm	Various	0.3	0.3	0.3	0.3	0.3	0.25	0.25	0.2
Solder joints ; primary side	No. joints	Telecoms Product	25900	27960	28520	29440	28980	31280	30170	31280
Solder joints ;secondary side	No. joints	Telecoms Product	4600	6900	5520	7120	6440	7720	6900	8096
No. of discrete components	Total Parts	Telecoms Product	1500	1680	1748	2024	2116	2200	2180	2460
Max. array components	Total Parts	Telecoms Product	48	80	64	80	81	12	96	128
Max. Peripheral components	Total Parts	Telecoms Product	96	128	110	128	120	144	120	144
SOME LIMITED COMPARISON WITH PREVIOUS IPC TECHNOLOGY ROADMAPS										
	2011				2009					
Leads/Component	Increase 16% over 6 to 10 years				Double over 8 to 10 years					
Max.No. of leads/component	Increase 110% over 6 to 10 years				166% increase over 8 to 10 years					
I/O pitch array packages	Reduce 40% over 6 to 10 years				Halve over 8 to 10 years					
I/O pitch peripheral array Packages	No change				Reduce 20% over 8 to 10 years					
No. of solder joints	Increase 30% over 6 to 10 years				Double over 8 to 10 years					
No. of discrete components	Increase 45% over 6 to 10 years				66% increase over 8 to 10 years					
Max. array components	Increase 200% over 6 to 10 years				350% increase over 8 to 10 years					

Key: RCG 1 Revenue Centre of Gravity (where most money is being spent)
SoA 2 State of the Art

Table 3 – PCB capability

PCB TECHNOLOGY FACTORS			Current 2010-2011		New Term 2012-2013		Mid Term 2014-2016		Long Term 2016-2020	
TECHNICAL DRIVER	METRIC	EMULATOR	RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Material Type		Telecom Module	FR4	Teflon	LowDk	LowDk	LowDk	LowDk	LowDk	LowDk
Board Thickness	mm min.	Consumer Interposer	0.4	0.6	0.5	0.4	0.45	0.35	0.45	0.35
Layer count	No.	Telecom Module	6	8	8	10	8	10	10	12
Embedded component	No.	Consumer Portable	0	0	0	0	10	16	10	16
Conductor width/separation	µm min internal	Telecoms Interposer	50/50	50/40	40/35	40/35	25/25	25/25	25/20	25/15
Hole dia.(through via)	µm min	Consumer Interposer	150	150	125	140	150	100	150	100
Land dia.value add to hole	µm	Consumer Interposer	200	180	180	175	180	150	180	150
Drilled hole for blind/buried	µm min dia.	Consumer Interposer	125	115	100	115	100	75	100	75
Microvias	µm min dia	Consumer Interposer	100	90	75	90	75	50	75	50
'Keepout' zone	Plus to land dia. µm	Consumer Interposer	300	250	300	250	275	225	250	200
Soldermask registration	Dia.µmWRT true position	Consumer Interposer	100	75	75	50	75	50	50	50
PTH aspect ratio	Max.	Automotive	4:1	4:1	4:1	4:1	5:1	5.3:1	6.9:1	10:1

SOME LIMITED COMPARISON WITH PREVIOUS IPC TECHNOLOGY ROADMAPS		
	2011	2009
Layer count	66% increase over 6 to 10 years	Double over 10 years
Embedded components	Anticipated next 2 years (2014)	Earlier Introduction
Conductor geometry	50 µm to 25 µm within 2 years	. . .
Land diameter	10% reduction over 6 to 10 years	50% reduction over 7 years
Blind/buried hole diameter (mechanical)	20% reduction over 6 to 10 years	40% reduction over 7 years
Microvia diameter	25% reduction over 6 to 10 years	25% reduction over 7 years
Soldermask registration	Allowance halved over 6 to 10 years	Allowance halved over 7 years

Key: RCG 1 Revenue Centre of Gravity (where most money is being spent)
SoA 2 State of the Art

Given the predicted design and assembly drivers, future demand on PCB capability may not seem proportionately onerous; albeit it will prove difficult enough. Ever finer geometry and the demands which that then places on registration appears to be the most significant challenge. Perhaps it is semiconductor devices that will have to take the biggest hit.

I admit to being sceptical about predicting the future of PCBs. I recall a 1980s PCIF event which we hosted at BT when a colleague foretold of the imminent demise of PCBs and the rise of hybrid microcircuits. Every five years I am told that the traditional subtractive/ additive process has reached its limit and that fully additive is the future. Maybe one day? Predictive data can never be one hundred percent accurate, but the IPC Roadmap is probably the best indicator we have of industry sentiment and the direction of travel. I now need to read the 85% of the Roadmap that I have only skimmed-over to date.

Roadmap data reprinted by kind permission of IPC. Further details can be found at http:/ / www.ipc.org/ roadmap

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3D Packaging Seminar

TWI, Granta Park, Abington, Cambridge, - 23rd May2012

Martin Goosey– ICT Chairman

On May 23rd 2012 TWI hosted a seminar on 3D packaging at its' conference centre in Granta Park, Abington, Cambridge. Organised by NMI with support from iMAPS and the Innovative Electronics Manufacturing Research Centre (IeMRC), this network event had the objective of presenting delegates with details of the latest technology roadmap developments, as well as information on the challenges and opportunities associated with 3D packaging.

The seminar began with an introduction and welcome by **Paul Jarvie** of NMI who thanked TWI for hosting the event and the IeMRC and iMAPS for providing additional support. He then introduced NMI, which was a trade body for electronics in the UK with over 220 members and whose activities encompassed all aspects related to semiconductor technology. Paul also highlighted NMI's involvement in the 'Electronic Systems – Challenges and Opportunities' (ESCO) Report (see http://www.esco-report.com) and Power Electronics UK. He also referred the attendees to a 'power electronics capability directory' which mapped the UK power electronics supply chain capability. Additionally, NMI was active in the Automotive Electronic Systems Network and supported the UK Electronics Skills Forum, which aimed to encourage the best talent to become involved in electronics and which was helping to address the diminishing skills capability in the UK. He concluded by giving a brief overview of the IeMRC funded FAMOBS project that was being led by Heriot Watt University.

The first technical presentation was then given by **Andrew Richardson** from Lancaster University, whose talk was entitled 'Inside 3D Packaging Technology'.

Andrew began by giving an overview of his packaging related work at Lancaster, which included engagement in multi-partner European projects around MEMS packaging. He then discussed the challenge of achieving best functionality without limiting performance in the context of integrating MEMS type devices. MEMS packaging had additional demands as it often required the interaction of the MEMS device with the environment. This meant that there was a need for more interfaces, which had to be addressed in terms of ensuring overall system reliability was achieved.

He then covered the effects of packaging materials on the functional performance of MEMS type devices. Thermal expansion mismatches between different materials were a common cause of reliability problems and, in 3D packaging, the substrate was often part of the overall package. There were also many other integration challenges such as provision of interconnects, choice of materials, need for self-testing and self-monitoring and the design itself; design for X was crucial for future MNT integration.

Andrew then gave an overview of some MEMS application areas and examples included pressure sensors, gas sensors, flow sensors, gyroscopes and optical sensors. He described the environmental challenges that had to be accommodated by electronics and illustrated the demands that had to be met in automotive applications.

The market drivers for 3D packaging were then outlined. These included increased functionality per unit area, more I/Os and higher operating speeds. The packaging hierarchy was also described and this ranged from wafer level packaging through multichip modules up to system level packaging. The example of wafer level packaging was described in detail and its advantages and disadvantages were defined. WLP offered the advantages of being able to test at the wafer level, as well as small package size and weight, direct chip attachment to the wafer and improved electrical and mechanical performance. It was noted, however, that plastic encapsulation could cause stresses in the semiconductor substrates and related reliability problems.

3D packaging of semiconductor die into a package was typically described as an example of Level 1 packaging. Examples of work that had been done in this area were then given and Andrew referred to a project called 'DAVID IST – 027240', which had down-scaled the assembly of vertically interconnected devices. This was an EC supported project and more information was publically available.

Finally, Andrew stated that there was a packaging roadmap that contained a lot of useful information and this was available from Marc Desmulliez at Heriot Watt University.

Chris Rider from the Cambridge Integrated Knowledge Centre (CIKC) then covered the subject of 'Integrating Large Area Electronics with Silicon – a new packaging challenge'.

He began by outlining the activities of the CIKC in Cambridge related to large area electronics and this included the use of new functional materials in applications such as lighting, photovoltaics and flexible displays etc. The best performance in this area was likely to come from the attachment of chips to flexible substrates. However, there were many challenges, not least of which was achieving reliability.

There were many so called 'brand enhancement opportunity' applications for this type of technology. Interest was growing in attaching bare die to flexible substrates, but this currently had even more challenges, especially as flexibility often had to be maintained and the typical substrate materials used could not be heated to high temperatures eg during die attachment.

Chris was working on an EPSRC proposal to establish a Centre for Innovative Manufacturing in large area electronics. He encouraged those with an interest to contact him at chris.rider@eng.cam.ac.uk.

The next speaker was **Per Viklund** of Mentor Graphics who gave a presentation on 'Advancements in 3D Packaging – pushing the limits of traditional EDA tools'.

He began by outlining the evolution of IC packaging and covered routable substrates, flip chip die attachment, multi-device packages and through silicon vias. He then went on to describe the complexity of the off chip interconnect network across multiple dies and the need to optimise the design of the interconnects to give best signal flow and hence performance.

Per stated that 3D stacking was not new in terms of packaging design and that the design tools had already been modified to support 3D. For some designs, the use of 2.5D interposers was a viable alternative and it offered a lower risk migration path towards a full 3D IC approach. These interposers could be both active and passive devices, the active interposers containing device layers as well as metal layers. The use of silicon interposers enabled TSVs to be moved off of the active die and also enabled the integration of passive devices. They were also compatible with older established wafer fabs.

Per then outlined the tasks that had to be undertaken in terms of the physical design and modelling required to develop a silicon interposer. This was a particular challenge as pin counts for some overall package designs could be in the region of 100,000 or beyond. The real solution to this approach required a cross-domain, co-design methodology encompassing the die, package and board levels.

He concluded by saying that here was a need to achieve an industry standard in interposer design and cross domain design tools were now required more than ever.

The final speaker in the morning session was **Keith Strickland** from Plessey Semiconductor and his presentation was called Packaging – an EPIC Story.

He began by detailing the history of the Plessey Company and its current activities, which included manufacture of EPIC sensors, high brightness LEDs and smart lighting. The company's core skill was in process technology. The focus of the presentation was on the EPIC sensor, which had been developed at the University of Sussex.

EPIC was a highly sensitive electrometer that operated in both remote and contact modes. It had many uses including health and fitness applications and could be built into smart phones, sports watches and single arm ECG monitors. There were also applications in the automotive sector, as well as in toys and games. In all of these applications, reliability was very important. Another interesting application was in imaging the latent charge from fingerprints, which decayed with time.

Keith then detailed the design of the EPIC sensor and the challenges in fabricating the device, especially in terms of integrating the sensor electrodes with the electronics. The packaging of the device was shown and a hybrid PCB based design had been evaluated along with a ceramic packaging approach. However, a QFN package was ultimately developed and the process flow was described.

The EPIC product roadmap out to 2016 was then presented and this included a move to a 0.18 micron process, the introduction of low power versions along with the development of sensor arrays and micro-arrays.

After a lunch and networking break **Alastair McGibbon** gave a presentation on NMI's R&D Policy Support. Alastair outlined how NMI worked with the funding holders in the UK to influence and support calls for proposals that would benefit the industry. NMI also helped with the transfer of know-how to build a presence around funding calls and to help partners to become involved. He then explained the many potential types of funding that were available and showed a funding map which highlighted the range of funding schemes at the regional, national and European levels. NMI were involved in the Advanced Manufacturing Supply Chain Initiative and it was seeking to encourage involvement from industry in this activity.

The second presentation of the afternoon session was given by **Ollie Althorpe** of ST Microelectronics Ltd and was on the subject of 'Interconnect for 3D Technologies'. ST Micoelectronics was a large multinational organisation with 300 people and three R&D centres in the UK.

Ollie stated that 3D packaging really came under the 'More than Moore' category. He then described the use of through silicon vias in camera applications which, in the case of ST Microelectronics products, ranged from VGA to 24 megapixel devices. Unlike with normal silicon devices, where Moore's law was a driver, for cameras, size reduction was constrained by the wavelength of light and the number of photons impinging per unit area. Therefore, alternative size reduction approaches were needed and the use of through silicon vias allowed the use of smaller outline packages with no pad extensions needed and an overall reduction in size. The use of TSVs also allowed the fabrication of camera modules that could be assembled via pick and place technology.

Ollie then showed a series of schematics describing the processing steps for the camera modules. The company had shipped hundreds of millions of these devices and reliability had been very good.

He concluded by stating that, in order to be successful, the whole process needed to be fully integrated and that one should only consider the use of 3D packaging approaches if no other viable routes were available!

The final presentation of the day was given by **Martin Goosey**, Industrial Director of the UK's Innovative Electronics Manufacturing Research Centre (IeMRC).

Martin's presentation was entitled Technology Developments in 3D'. After giving an overview of the IeMRC and its packaging related research work, he described the current status and the likely progression in 3D packaging technology towards assembly at the wafer level and highlighted the benefits that 3D packaging could offer.

He also detailed the issues associated with 3D packaging and then focussed on the challenges around thermal management in these highly integrated package types. In the final part of his presentation Martin described the possibility of using nanotechnology and nanomaterials as one way of overcoming the problems with heat and its dissipation in 3D packages.

Materials such as carbon nanotubes and graphene had thermal conductivities of several thousand W/mK and, in theory at least, offered an order of magnitude improvement in thermal conductivity over more conventional materials such as aluminium nitride.

Martin also explained that carbon nanotubes had been proposed as alternatives to copper in through silicon vias, where they offered the benefits of higher electrical and thermal conductivity along with a simpler deposition process.

He concluded by outlining the IeMRC's forthcoming events and invited attendees to attend them.

This was an excellent event that combined a wide range of varied and interesting presentations with a networking opportunity for the delegates. NMI are to be commended for organising such as successful event.

Martin Goosey
23rd May 2012

***Speakers and sponsors**; L to R: Andrew Richardson, Keith Strickland, Martin Goosey, Alastair McGibbon, Ollie Althorpe, Andrew Holland, Matt Brown.*

Research to Industry Electronics Conference: Connecting Research to Industry

Henry Ford College, Loughborough -19 June 2012

Martin Goose– ICT Chairman

On 19th June 2012, around 100 delegates attended the Henry Ford College in Loughborough for the first **"Research to Industry Conference: R2i".** The aim of the event was to enable academic researchers to network with industrialists and forge new links that could help move their work from academia towards commercial exploitation. To that end the event had been structured around a series of 35 short presentations from the researchers. Coupled with this, each of the four sessions was opened with a keynote presentation offering advice and guidance from people actually involved in taking research into industry. There was also a wide range of posters providing additional information and table top exhibits from industrial sponsors.

Darren Cadman

Andrew Holland

Darren Cadman of the IeMRC welcomed attendees to the R2i Conference which had been organised by the Innovative Electronics Manufacturing Research Centre (IeMRC) and iMAPS, with support from the IEEE, the ESP KTN and NMI. **Andrew Holland** of iMAPS also then welcomed the attendees and announced the award that his organisation would be making to the best project presented at the conference.

Next, the industrial exhibitors were given the opportunity to make a short presentation on their organisations. These included Inseto and Tecan, as well as representatives of the High Value Manufacturing Catapult and the Knowledge Transfer Partnerships.

Darren then gave an overview of the activities of the IeMRC, which was one of 16 such centres and was established in 2004. The IeMRC was funding research projects across the UK with support from the relevant industry supply chains, as well as organising workshops, seminars and conferences. The next IeMRC call for proposals was said to be imminent. The work that the IeMRC supported had to be of high quality and impact with its research being subject to international review. The IeMRC was also undertaking a review of the UK's electronics research needs for the EPSRC.

Alistair McGibbon of NMI then gave an introduction to NMI followed by an overview of the mechanisms that were available for the funding of research projects, the pathways and requirements. He gave an overview of the R&D journey and stated that it was important to choose the right R&D activities, so that they fitted the needs of strategic business development. The huge range of potential funding routes was also outlined.

Following the initial opening presentations, the main part of the day was dedicated to a series of five minute presentations covering a wide range of research projects being undertaken at universities around the country.

The first pitch of the day was from **Dr Hazel Assender** of Oxford University, who covered the IeMRC funded flagship project on roll to roll vacuum web coating, called RoVacBe. RoVacBe was investigating the roll to roll deposition of organic semiconductors, metals, oxides and polymers on organic substrates. Web speeds of up to 5 ms^{-1} had been achieved with web widths of up to 350 mm. The project work to date had achieved the high speed roll to roll deposition of organic transistors, transparent conducting layers, and the other materials required to make functional devices. The team was also working extensively with industry via the industrial partners supporting the project. They were looking for ways to take the technology into new areas such as photovoltaics and they would welcome further research collaboration opportunities.

Axel Bindel

Next was a presentation on a TSB supported project called InBoard given by **Axel Bindel** of Loughborough University. InBoard used RFIDs incorporated into multilayer printed circuit boards to store relevant information within the product with the potential to provide monitoring throughout the whole product lifecycle i.e. from manufacture to end of life. Such products with this type of stored knowledge about manufacturing and utilisation could be used to increase quality, reliability, service and resource efficiency. The information was accessible at the point where the product was located, for example, on the shop floor, across the supply chain, during use and at the end of life recycling stage. The project had successfully embedded RFIDs into multilayer PCBs and the accompanying processes, software architecture and interfaces had been developed.

Liudi Jiang from Southampton University then described work on another IeMRC supported project and one that was researching carbon nanotube composite surfaces for electrical contact interfaces. MEMS-based contacts had a number of advantages including fast switching, tolerance of high G and small geometries. An aim of the project was to fabricate advanced electrical contacts for MEMS relays with significant performance and manufacturing potential. In particular, prototype MEMS switches were needed that were capable of switching >10 mA at up to 4 V over $>10^8$ cycles. MEMS switch/relays had been forecast to be a multibillion dollar technology area but technical barriers were the lack of switches and the need for high conductivity, reliability and long lifetimes. CNT based devices could provide extended switching cycles compared to more conventional switching and had small geometries for RF applications. Work to date had demonstrated that, by using a carbon nanotube surface, it had been possible to switch 20 mA at 4 V for more than > 80 million cycles. The researchers were looking to secure follow on funding from the TSB, or possibly the EC, and would welcome contact from industrial

collaborators with experience in MEMS manufacturing and related packaging.

High frequency flexible fabric electronics were then described by **Yiannis Vardaxoglou** from Loughborough University. This project, which also included Nottingham Trent University and several industrial partners, was investigating the concept of using conductive threads to fabricate electronics including antennas for numerous applications. The aim was to find the most effective way to produce fabric antennas and their associated electronics and to integrate them into fabric. There were many applications for the technology such as in search and rescue, defence, healthcare, sport and leisure and aerospace. Current monopole antenna solutions for search and rescue applications were described as being clumsy, big, ugly, obtrusive, prone to breakage, easily forgotten and difficult to operate in emergencies. There was thus plenty of scope for innovation. The feasibility of using digital embroidery and conducting threads to create RF transmission lines had been demonstrated and an assessment of the conductive threads completed. Patch and dipole antennas had been designed, fabricated and evaluated, comparing well to their copper-based equivalents. The current technical focus was on performance under extreme conditions and scalability. Target applications had been identified and there had been interest from the industrial partners.

Wayne Cranton of Nottingham Trent University then discussed his work on photonic processing of thin film electronic materials including metal oxides and metal sulphides using UV pulsed laser processing. The work was focussed on thin film deposition and characterisation and included the use of pulsed UV-laser processing. There was also work on the processing of inkjet printed thin films. The aim was to enhance properties such as conductivity, mobility and stability etc for use in plastic and printed electronics, phosphor sensors, security materials and other applications. A particular interest was in optically transparent conducting materials. The group was also involved with two TSB funded projects; one called HESSLIS to develop transparent conductors on plastic and the other called Fab3D which was working on the printing and processing of nanoparticulate layers for electronics and displays.

The second session was opened by **Andrew Darwent** of the Knowledge Transfer Partnerships which were managed by the Technology Strategy Board. KTPs were described as a mechanism for providing a commercial pull to research carried out at Universities. KTP projects typically lasted from 6 months to 3 years, with 2 years being the preferred duration. The associate worker on a KTP project would be jointly recruited but employed by the knowledge base partner and typically located at the business premises. KTPs required innovative projects with a strategic relevance to the business and that had a clear knowledge transfer element creating a step change in capability. Some examples of successful projects were then shown, including one on GPS software development with DeMontfort University.

The technical presentations recommenced with **Jeremy Everard** from the University of York covering his work on high speed electronics and optoelectronics. His focus had been on low noise oscillators and research to make them more compact and robust. A wide variety of low noise oscillators had been developed, some of which showed the best performance available anywhere.

Andrew Holmes from the MEMS/Microsystems Group at Imperial College, London then discussed his IeMRC funded work on thermosonic adhesive flip chip assembly for advanced microelectronic packaging. The aim of the project had been to improve the performance and reliability of adhesive assemblies using thermosonic bonding. He described his group's laser microfabrication capabilities, which included an excimer laser mask projection system and a DPSS laser salvo-mirror scanning system. Application areas embraced work on MEMS, lab on a chip, thin film patterning, microvia drilling, mask and IC repair, ink jet printer nozzle drilling, catheter cutting and many others. Andrew was seeking new industrial and academic partners for future collaborative research work in the areas of flip chip technology and laser microfabrication.

David Hutt of Loughborough University then detailed his group's work on copper filled conductive adhesives for printed circuit interconnects. The research had a focus on using electrically conducting adhesives for interconnects and was seeking to replace traditional expensive silver particles with copper. This was difficult because of the propensity of copper to oxidise. The problem was overcome by treating the copper particles' surfaces with a self-assembling monolayer layer that prevented oxidation. Using these materials offered a potential saving of more than 100 times compared to silver. Examples of circuits were shown and their low temperature processing gave compatibility with a wide range of polymer substrates.

Tony Corless from the Advanced Technology Institute at the University of Surrey then discussed his work on the use of focussed ion beams as a nanomachining CNC tool. This approach had been used to produce master tools for a range of masks and related products such as nanosquid devices. It had also been used for the production of master tools for the embossing and moulding of lenses, gratings and roughness standards at scales and accuracies that were not accessible using conventional machining. A key aim for the future was to scale up the process and new inputs from interested partners were sought as this could help with the determination of the optimum resolution versus output.

John Graves from Coventry University then described a new collaborative project with Loughborough University which was on the functionalisation of metallic nanoparticles to enable metallisation in electronics. This was described as offering a novel approach to the metallisation of non-conductive substrates eg PCBs and MIDs. It aimed to offer a more cost-effective utilisation of materials and improved adhesion properties. The intention was to use copper nanoparticles as an alternative to the Sn/Pd catalysts that were typically used in electroless metallisation applications, thereby reducing the use of precious metals which suffered significant price and availability fluctuations. Proof of concept had been demonstrated and the work could potentially lead to significantly lower costs while having applicability to a wide range of substrates. The project was looking to engage with end users of the technology who had experience with a range of substrates other than FR4, as well as those with expertise in particle analysis and nanoparticle dispersion.

Next, **Rehana Kausar** from Queen Mary University, London talked about her work on quality of service and the use of packet switching in wireless communication networks. This could provide low cost services for end users and operators, while offering improvements in quality of service for both operators and users.

Christian Klumpner from Nottingham University then discussed his work on characterisation, emulation and power management of supercapacitors and batteries. The university had expertise in the design of power electronics systems to interface energy storage to various applications e.g. power grid, renewables and transportation. There was also expertise in the characterisation of various energy storage devices from a user's point of view. The work would also enable the implementation of emulators for novel energy storage components that could provide information on scale up behaviour for system prototyping and testing. This research had relevance to renewable energy, transport and distribution of electrical power, as well as to hybrid and electric vehicles.

David Watson from MISEC at Herriot Watt University presented his work on laser direct writing of metals on plastic substrates such as polyimide. He described a patented chlorophyll-based process which used a material that was natural and abundant and that didn't require any photoresists or imaging stages. It also had low equipment costs and avoided the use of etchants and the generation of the typical associated wastes. The process provided a fast turnaround time enabling the production of small volumes of customised products and rapid prototyping. It could be used on flexible sheets and coated contoured surfaces. There were many market opportunities, such as in the areas of printable power, light intelligence, sensor and products with embedded, wearable and invisible technologies. Demonstrators had been produced and the process had been characterised. The next stage was to manufacture some prototype functional devices. The group were looking for industrial partners to help move up the technology readiness levels so that the process could be transferred into industry.

The final presentation of the morning sessions was given by **Maria Mirgkizoudi** from Loughborough University and it was on reliability studies of microelectronic interconnects in harsh environments. This was a study of electronics performance in combined environmental conditions and involved the development of testing systems and methodologies for qualification testing. The project goal was to develop testing systems capable of undertaking reliability tests on microelectronic packages under combined thermal and mechanical loadings in harsh environments. Key challenges included the knowledge gap and lack of supporting hardware and software in testing and qualification of electronics under such harsh conditions and the fact that the fundamentals of the resulting

device/component failure mechanisms did not exist. The work included metallurgical studies on the critical areas of wire bonded devices to identify areas of susceptibility.

There then followed a networking lunch which gave the delegates the opportunity to reflect on the wide range of research subject matter that had been presented during the morning, as well as to visit the poster and exhibitor areas to learn more about specific topics of interest.

Nigel Rix of the ESPKTN opened the first of two afternoon sessions and introduced **Martin Goosey**, Industrial Director of the IeMRC, who gave a presentation entitled 'From Research to Industrial Implementation – the journey of a successful project'. Martin began by outlining some of the key challenges of taking research up the technology readiness levels towards commercial implementation and he discussed the so called 'valley of death' which had proved a stumbling block for many good technologies when attempting this transition. He also mentioned that the UK government had now acknowledged the need to get more of the UK's successful research into industry, where its benefits could be utilised and he cited, by way of example, the recent announcement of substantial funding to support the development of graphene in the UK.

Martin then moved on to describe the path that one of the IeMRC's own projects had used to take it from basic research to commercial exploitation. The project detailed was initially undertaken by Coventry University and involved the use of ultrasonics to reduce energy and chemical consumption in the PCB fabrication process. The success of the initial research had led to a Technology Strategy Board funded feasibility study that allowed the technology to be trialled on an industrial scale. Further positive results had then encouraged the team to apply for European Commission funding for a first implementation project under the Eco-Innovation scheme. The resulting three year 'Susonence' project would result in the manufacture of five industrial scale demonstrators, four of which would be installed in manufacturing plants in Paris and Prague.

Martin concluded by providing details of the various funding schemes that had been used and showing examples from where additional help and assistance was available.

Dr Anne Vanhoest from UCL began with an overview of her proposal for a Centre of Excellence for Medical Electronics Packaging (CEMEP). One of the important areas the centre would be involved with would be electronics reliability in harsh environments. Although the centre's primary interest sector would be around medical engineering, there would be also be involvement with other related industrial sectors and the centre was therefore looking for additional adventurous and creative partners.

Stewart Smith then talked about design research in the Institute for Integrated Micro and Nano Systems at the School of Engineering in the University of Edinburgh and the work of the CMOS Sensors and Systems Group. They were working on mixed signal and digital systems design, neuromorphic electronics, sensor interfaces and integrated microsystems. An example of work on CMOS single photon detector arrays was given along with a brief discussion of applications for time resolved sensors for biomedical imaging and sensing. Other research interests reported included work on new smart low power sensors.

Smart Design Research at Nottingham Trent University was then reported by **Philip Breedon**. This included rapid manufacturing technologies for smart materials and flexible circuitry for electroactive polymers and bio-sensors, the development of artificial muscles and bio-compatible additive manufacturing. The group was looking for collaborators with expertise in a variety of areas including functional inks, silicones, flexible circuitry and power supplies for medical devices and artificial muscles.

Rhys Rhodes from the Advanced Technology Institute at the University of Surrey followed with a talk on 'smart hybrid organic photovoltaic structures: a novel concept for long term efficient energy generation'. The institute was working on the development of solar powered hydrogen generation for efficient energy management and also on emissions-free energy production. The research was looking into the use of a photoelectrochemical cells to split water into hydrogen and oxygen, and the subsequent removal and storage of the hydrogen for later use. This was seen as an area for expansion in the context of renewables. Proof of concept had been demonstrated using in-house graphinated nanostructures as photocatalysts and platinised TiO_2 deposited on a commercial photovoltaic cell, with the next step being to produce a completely self-contained prototype.

Stoyan Stoyanov from the Mechanics and Reliability Group at the University of Greenwich was next with 'Digital tools for DfX'. The group had skills and technology in virtual prototyping, multi-physics techniques, reliability/failure modelling, robustness validation, and risk analysis. Its research focus was on integrated models for DfX, physics of failure and reliability, process modelling and prognostics and health management and was of value in defence, aerospace and other high reliability and safety equipment. A recent example project had been the technology assessment of the effects of refinishing lead-free microelectronic components.

Brunel University's work on power biomedical and self-powered smart electronics was then described by **Tony Vilches.** Their group had a focus on novel, flexible electronic materials and low power smart electronic devices and systems and their work was aimed at creating novel electronic materials with tailored piezoelectric/thermoelectric/super-capacitive properties for use in new biosensors and energy harvesting systems. Current work also included research on biofuel cells for in-vivo use (see for example the following paper; CNT fibre based glucose sensor, , , 21, 16501).

Finally for this session, **Gavin Williams** presented work being carried out jointly at the Universities of Sheffield and Durham on 3D lithography. The problem when undertaking 3D lithography was that diffraction limited resolution when using a mask and the effects became worse with non-planar substrates. The approach being developed by these two universities employed a laser illuminated computer generated hologram which was used in conjunction with a conformal photoresist. A number of application examples were shown including microstructured silicon and 3D antenna structures. The technology was cost effective for mass production and could be used for patterning non-planar substrates.

The final session of the conference was opened by **Alan McClelland** from the Centre for Process Innovation (CPI) and he began by giving a talk on the electronics capability in the High Value Manufacturing Catapult Centre. He described the evolution of the centre and referred to two influential reports that had been produced by James Dyson and Herman Hauser. These reports had highlighted the problems of getting new technology to market and the Catapult Centres were aimed at bridging the gap (the valley of death) between academia and industry with the Centres working at the TRL 4 to 6 levels. The printable electronics facilities at CPI were also detailed and these included 1000 m^2 of class 100 and 1000 clean rooms containing a wide range of automated processing equipment.

The first short presentation of the final session was given by **David Harrison** from Brunel University's Cleaner Electronics Group and was entitled 'of the environmental impact of printed and plastic electronics applied as smart packaging'. David gave an overview of his group's research facilities and capabilities and discussed the challenges around smart packaging and the need for more resource efficient designs for printed electronics. Current projects included 'Powerweave' which was researching energy generation and storage on textiles. The challenges around smart packaging were also mentioned and included what happened when highly visible, highly distributed packaging materials moved from being compostable materials to electronic waste. Another question was whether more resource efficient designs for printed electronics could be developed. Brunel was investigating this area via a TSB funded project called BEDS (biodegradable electronics). Smart packaging was an area where very large market growth was projected, but little work had been carried out to date to consider the potential impacts associated with the uptake of this new technology.

Stewart Smith returned to discuss microsystems research at the University of Edinburgh. The facilities available were described and these included class 100 clean rooms for processing 200 μm substrates. The work involved the development of post-processing for microsystems integration. An example was shown of liquid crystal on silicon micro-displays (LCoS) which had been taken forward by Forth Dimension Displays. There had also been work on magnetic components made using thick electroplated metals for inductors. Digital microfluidics work was also described, this involved moving discrete droplets of liquids via the use of two different technologies: these utilised either an electrowetting on dielectric (EWOD) approach or the use of Surface Acoustic Wave (SAW) filters. There had also been a long history of microelectronics

test activity and metrology and the current focus was on MEMS and microsystems.

Richard McWilliam form Durham University then discussed the work of the EPSRC Centre for Innovative Manufacturing in Through-life Engineering Services. Its interests included self-repairing electronics and related mechanisms that extended component lifetime and maintained critical operations.

Derek Sinclair continued the session with 'Functional Oxides at Sheffield'. The group at Sheffield had more than 50 researchers and their work was aimed at the development of functional oxides for antennas, thermistors, actuators, Li-batteries, fuel cells, thermoelectric, memristors and several other applications. There was, for example, a need for lead-free electro-ceramics and they had developed multilayer actuators using a high Tc piezoelectric multilayer actuator. The department had facilities and expertise from fundamental science to the production of prototype devices. Examples were shown of the oxide-based multilayer actuators that were used in the fuel injection systems of modern diesel engines.

Darren Southee of Loughborough University discussed his work on product design for printed electronics with integrated power sources. He covered his current work at Loughborough and his previous work at Brunel on lithographically printed conductors, batteries and thermochromic displays, showing examples of printed interconnects, displays and battery structures. He also described the product design of a heated container that was used for keeping corn snakes at a specific required temperature.

Samjid Mannan from King's College, London reviewed his work on radically new solder materials for applications up to 185°C. These new solder pastes were based on SAC but with the addition of coated zinc particles that dissolved into the solder during reflow. This material showed good reliability during storage at 150°C for 1000 hours and temperature cycling from -20°C to 175°C over three hundred cycles. There was also evidence that the solder could withstand environments of 185°C using nickel substrates and component terminations for extended periods of time. Current results had shown reduced IMC formation and higher reliability for both copper and nickel terminations, but post reflow cleaning was required. The new paste was expected to be of interest to electronics manufacturers involved in oil/gas drilling, as well as those supplying the aerospace, power electronics and automotive sectors. The project was due to finish in December 2012 and interested parties were needed to evaluate the solder pastes in their own applications. Other related work at King's included work on high melting point lead-free solders for applications up to 260°C and on nanoparticle copper sintered joints for applications above 300°C.

Wenhui Song from Brunel then discussed work on the screen printing of carbon nanotubes for field emission devices. This involved the production and functionalisation of carbon nanotubes, graphene and graphite nano-sheets, along with the formulation and characterisation of carbon nanomaterial-based inks and the screen and inkjet printing of carbon nanostructure field emitters, electrodes and devices. Current thermionic cathode-based electron sources used hot filaments and were bulky and energy inefficient. Field emitter devices, conversely, were energy efficient cold cathode devices. The main challenge had been to develop a cost effective industrial approach to achieving high current electron emission of carbon nanomaterials and, to date, promising results had been achieved.

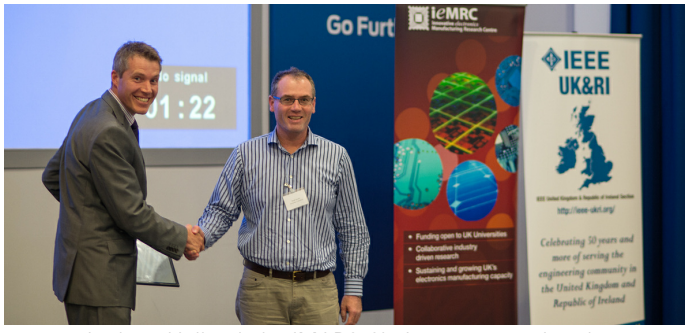
Dr Bala Vaihyanathan of Loughborough University's Department of Materials outlined work on the microwave assisted processing of multilayer electroceramic devices (ECDs). Conventional processing of ECDs was tedious, time consuming, energy intensive and required high temperatures. Problems that could be encountered included excessive grain growth, electrode migration, electrode delamination and interdiffusion of components. Work had been carried out to determine if microwaves could be used to overcome these problems. Microwaves offered volumetric and 'inside out' heating along with more rapid heating and cooling. Varistor ceramics prepared using microwaves exhibited a 23% enhancement in densification and superior electrical properties due to their finer grain size. In addition, the enhanced densification had been achieved in one tenth of the time normally required, along with a reduction in sintering temperatures, interfacial diffusion and electrode migration. The group was looking for collaborators for the development of new varistor and capacitor formulations, as well as partners that could help apply the methodologies for new systems and scale up.

The final technical presentation of the day was by **Geoff Wilcox** from the Department of Materials at Loughborough University, who discussed his research on tin whisker formation via the IeMRC funded Whiskermit project. He gave an overview of whisker formation and discussed the implications of the legislation driven lead-removal from alloys, which had caused renewed problems with tin whisker formation. Further miniaturisation in electronics had also made matters worse because whiskers were more easily able to bridge the smaller gaps between components and tracks etc. Also, at the lower voltages used, whiskers could sustain currents and cause problems. The Whiskermit project was using a dual approach to whisker mitigation; one being the modification of electroplating process and the other being the development and use of conformal coatings to retard whisker growth. The mechanisms of tin whisker growth on brass had been studied and the role of lead as a whisker mitigator in Sn-Pb electroplated finishes had been investigated. The project consortium was looking for new partners to join the project. There was also an interest in the electrodeposition of tin alloy solder finishes utilising non-aqueous ionic liquid formulations. Work was also planned to investigate the mechanisms for, and mitigation of, zinc whiskers on finishes associated with electronics.

At the end of the formal presentations **Nihal Sinnadurai** of the IEEE gave the results of the IEEE's assessment of the best projects presented during the day. He described the terms that had been used in making the choice and he also mentioned a number of specific projects, such as Anne Vanhoest's Centre of Medical Electronics Packaging, that the IEEE would support in the future. Liudi Jiang from Southampton, Hazel Assender from Oxford, John Graves from Coventry and Axel Bindel from Loughborough were awarded gifts from the IEEE for their excellent presentations. Andrew Holland, the iMAPS Chairman, then thanked all of the speakers for their high quality contributions and the IeMRC for its role in organising the event. He gave a brief overview of iMAPS and its activities before moving on to give the iMAPS award for the best project. This was a cash prize of £2,500 for use in taking the project forward and it was awarded to Derek Sinclair from Sheffield University for his work on functional oxides.

Overall, this turned out to be an excellent and novel type of conference that held the attention of the attendees throughout a very varied and interesting day by providing insights into the vast array of valuable electronics research that is being undertaken within UK academia and which has the potential to provide real benefits to the UK electronics industry. Based on the success of this event, it seems likely that further conferences of this type would not only be most welcome but of great use. The individual presentations from the conference are available on the IeMRC's website;

Liudi Jiang from Southampton University receiving her award for research into carbon nanotube composite surfaces



Andrew Holland, the iMAPS Chairman presenting the iMAPS award to Derek Sinclair from Sheffield University for his work on functional oxides

The elimination of whiskers from electroplated tin

by

George Milad

Introduction

As the implementation of the ROHS Directive continues to affect the electronics industry, tin and tin alloys remain the first choice for replacing conventional tin/lead alloys and lead-free soldering and solders are presently well implemented in the industry.

There is a good understanding of lead-free solders including the family of SAC alloys and the tin/copper alloy used for lead-free hot air solder levelling. The understanding extends to the type of inter-metallic compound (IMC) formed, its propagation and the integrity and reliability of the solder joint that is produced.

There is also a continuous effort to develop even better products that may lower the reflow temperature or reduce the IMC propagation for greater solder joint reliability and to give a wider assembly window. Some of these efforts involve adding small amounts of dopants to the presently used lead-free alloys.

On the surface finish side, replacing tin-lead has posed greater challenges. Component leads and connector finishes were being converted to tin as an obvious alternative. Tin is easy to apply, is readily solderable and is economic to use. Tin also works well as a soldering surface. However, any part of the lead or the connection surface that is not soldered to,has shown a propensity to form tin whiskers over the life of the part. Internal stresses in the deposit coupled with IMC formation along grain boundaries, as well as external stresses on the deposit, are known to initiate whisker formation.

A lot of time and effort has been directed at tin whisker "Mitigation". There are a series of methods to determine the propensity of a tin finish to form whiskers, as well as recommendations on how to evaluate the same. This paper describes two approaches that were successful in eliminating whisker formation. Both approaches dissipate the stress that is formed from the interaction of IMC formation and the inherent structure of electroplated tin. The first is to modify the substrate surface to control the growth in thickness and direction of propagation of the IMC and the second to modify the large columnar tin deposit crystal structure to mimic the fine equiaxed structure of tin-lead solder. Controlling the IMC thickness was achieved by micro-roughening the copper substrate before tin deposition. The modification of the crystal structure was accomplished by the use of specific organic additives that disrupt the columnar growth and give rise to smaller equiaxed crystals.

Electroplated pure tin and tin based alloys, are being used as alternatives to tin-lead in the majority of electronic components. These alternatives are known to produce tin whiskers which may give rise to short circuits on these components.

In the case of tin finish on copper and copper based alloys, the major cause of tin whisker formation is compressive stress. The stress is mainly caused by irregular growth of copper-tin inter-metallic compound (IMC) at ambient conditions [**1**]. It is known that tin whiskers are readily formed on electroplated tin deposits on copper and are not observed on electroplated tin-lead deposits. The tin deposit and tin-lead deposit are different in the crystal structure. Crystal Structure has a direct impact on tin whiskers formation [**2**] [**3**].

A tin deposit with modified crystal structure (similar to tin-lead deposits) is capable of preventing whisker formation by dissipating and delocalizing the stress that cause whiskers.

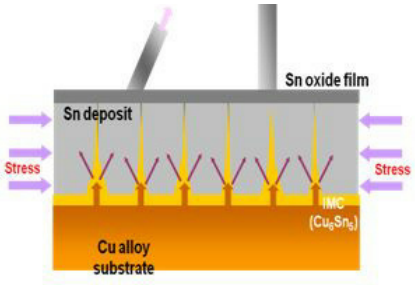


Fig.1 Shows a schematic of tin whisker formation.

As shown in Figure 1, stress, channeled along the boundaries of the large grained columnar tin deposit, is responsible for the emergence of tin whiskers. Stress may be internal or external (refer to figure 2). The primary source of internal stress is attributed to the non uniform increase in the thickness of the IMC layer over time at ambient conditions (e.g.30° C, 60%RH for 4000 hours). Another condition that produces internal stress is exposure to high temperature and high humidity (e.g.55°C ,85%RH for 4,000 hours) for extended periods of time which gives rise to

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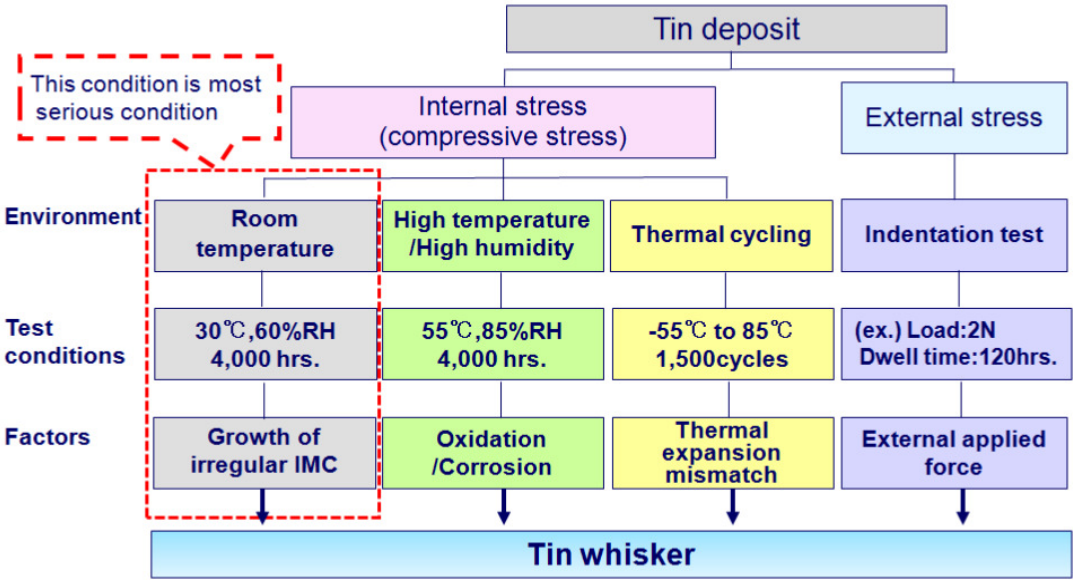


Fig. 2. Four different paths that lead to stress and whisker formation

oxidation and/or corrosion. Internal stress can also be induced by thermal cyclng (-55⁰ Cto 85⁰ C for 1,500cycles) due to omismatched CTE (coefficient of thermal expansion). The latter two forms are commonly used to induce internal stress in controlled experiments. External stress is also known to initiate whisker growth. An example is the stress induced by press fit connectors.

Experiments and Results

A. Copper Surface Modification

A study was conducted on the morphology of the copper substrate prior to plating. A series of substrates varying in roughness were evaluated for whisker formation after electroplated tin deposition. The roughness was controlled by chemical etching procedures. Average roughness "Ra", varied between 0.13 to 0.47 µm. As shown in fig.4, 0.47µm Ra has a much larger surface area as compared to 0.13µm Ra. The propensity to whisker was evaluated as follows:

Test Vehicle

The test vehicle was a CDA19400 (Cu-2.3Fe-0.03P-0.12Zn) leadframe; refer to fig. 3.

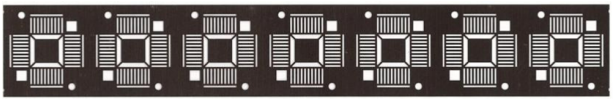


Fig.3 Leadframe Test Vehicle

Tin plating

The plating bath was methansulfonic acid based matte tin. The plating was run at a current density of 10A/dm². Plating time was varied to produce a 3 µm and a 10 µm thick deposit. The former was for short term whisker evaluation and the latter which is typical of lead frame plating was used for long term evaluations.

Methodology

The test vehicles were subjected to chemical micro-roughening to produce a set of specific Ra values (Fig. 4) The figure shows the SEM micrographs of the different degrees of micro-roughening as measured in Ra um.

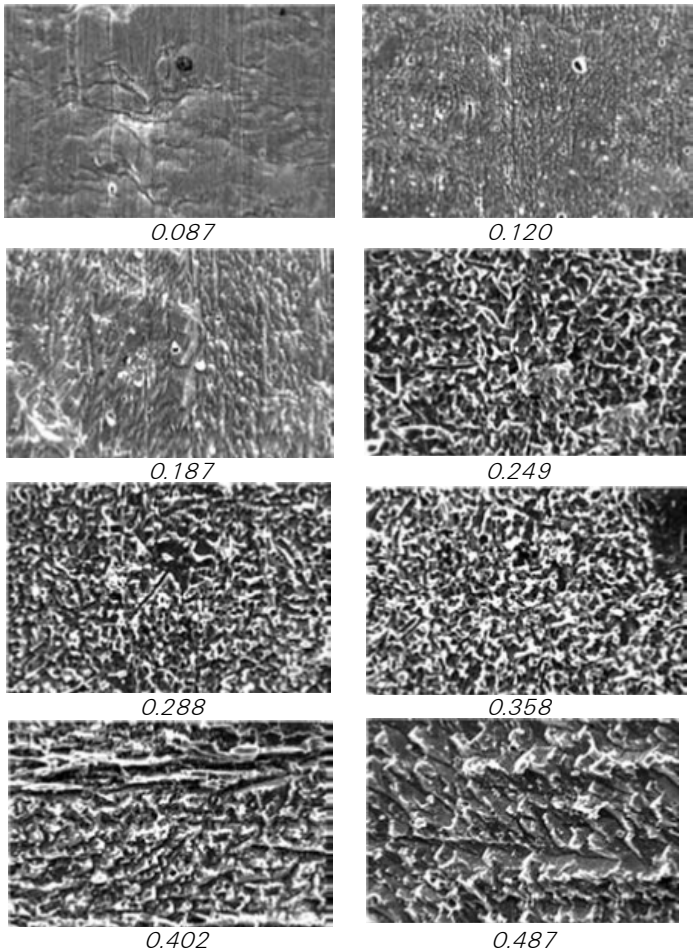


Fig. 4. SEM micrographs of different Ra values

The samples were then run thru a standard plating process as outlined in Fig. 5. The samples were then stored under controlled ambient conditions (30⁰ C/60%RH) for extended periods of time (1000 hours). The samples were examined for whisker formation at various time intervals.-

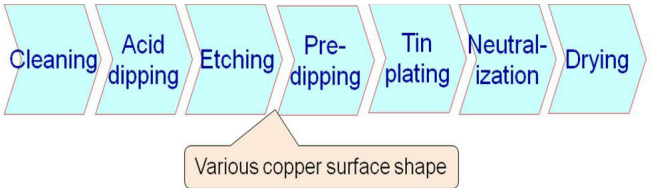


Fig.5 Showing theprocess used for this study (typical sequance)

Definition of a "Whisker"

A whisker is a protrusion >10 μm in length and that has an aspect ratio (length/diameter) >2.

Measurement of whisker length

The measurement according to JEITA ET-7410 is the straight line distance from the point of emergence of the whisker to the most distant point on the whisker.

Results and Discussion

Whiskers were examined, measured and tabulated after 1000 hours of storage under controlled ambient conditions (30° C/60%RH). The data gathered from whisker examination on the various morphologies of roughening are graphed in Fig. 6 and 7. Fig. 6 looks at maximum whisker length as a function of roughness. Fig. 7 shows the whisker density per mm2 as a function of roughness.

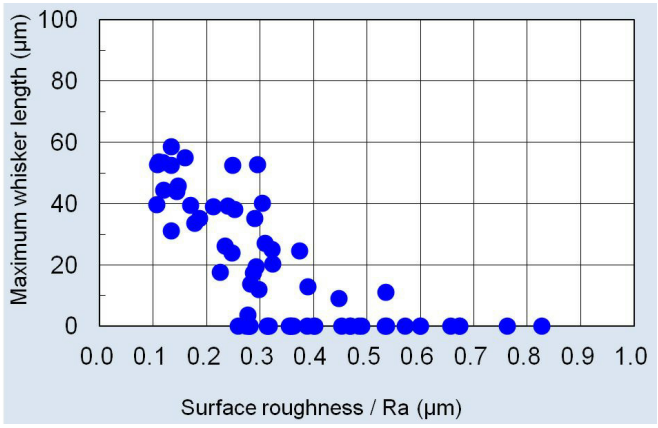


Fig.6 Maximum whisker length as a function of roughness

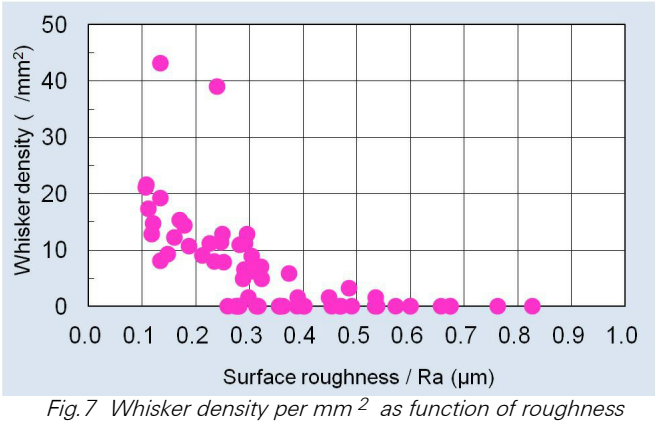
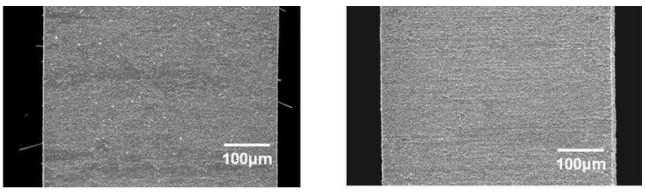


Fig.7 Whisker density per mm 2 as function of roughness

The data indicate that there is clear correlation between surface roughness and whiskering propensity. The rougher surface produces lower whisker length and also lower density per mm2 Fig. 8 shows whisker growth on 3 μm of tin plated on smoother copper (Ra 0.13) as compared to no whiskers on the rougher surface (Ra 0.47).

In an effort to explain these results, more work was performed. Samples with a tin deposit thickness of 10 μm were stored for 7,000 h at 30°C/60% RH. The tin was then stripped by chemical means and the IMC morphology was examined. In addition, cross-sections were prepared and examined to verify the top-down observation.



Ra 0.13 whiskers *Ra 0.47 No whiskers*

Fig. 8 3μm Tin after 1000 hours at 30 C/60% RH

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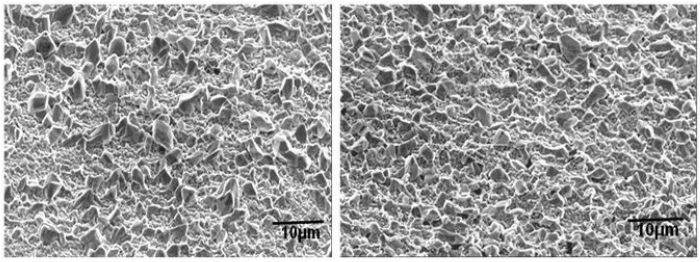


Ra 0.13 μm *Ra 0.47 μm*

Fig. 9 Morphology of IMC surface after stripping of the two extremes of Ra

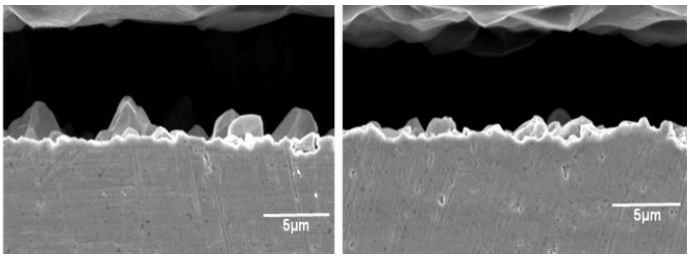


Fig. 10 shows cross-sections of the same Ra values.

It is clear that the rougher Ra of 0.47mm produced a thinner more uniform IMC, compared to the smoother Ra of 0.13 μm, which showed increased IMC thickness in localized areas. A plausible explanation is that the IMC is spread over a much larger area on the rougher morphology (Ra 0.47μm) as compared to the smaller area of the smoother surface (Ra 0.13 μm). It follows then that the stress resulting from IMC formation would be highly reduced and dissipated with increased surface roughness of the underlying copper substrate.

The solderability and the ductility of a 10μm tin deposit on the two extremes of surface morphology were examined using "Wetting Balance Testing" as well as via the "Bend test". There was virtually no difference in performance as can be seen in Fig. 11.

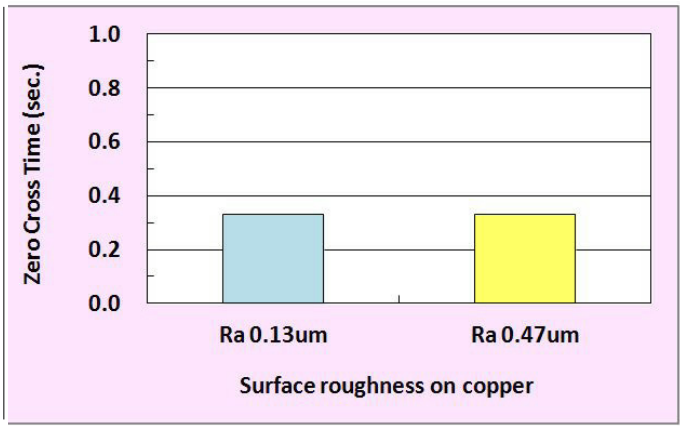


Fig. 11 Comparison of zero cross-time of 10 μm tin deposit for two levels of roughness.

B. Modifying the crystal structure of the tin deposit

A close examination of the crystal structure of both tin and tinlead alloy shows a clear difference between the two deposits. The tin-lead which does not whisker has an equiaxed relatively fine-grained deposit. The tin on the other hand shows larger columnar crystals. Fig. 12 shows the difference in crystal structure between tin and tin-lead alloy (10 wt% Pb). It is believed that, if the crystal structure of the tin deposit can bemodified to the tin-lead crystal structure, the stresses will be dissipated and whiskers will not form.

Tests were conducted using the same test vehicle and the same plating conditions as outlined earlier in the copper surface roughness study above.

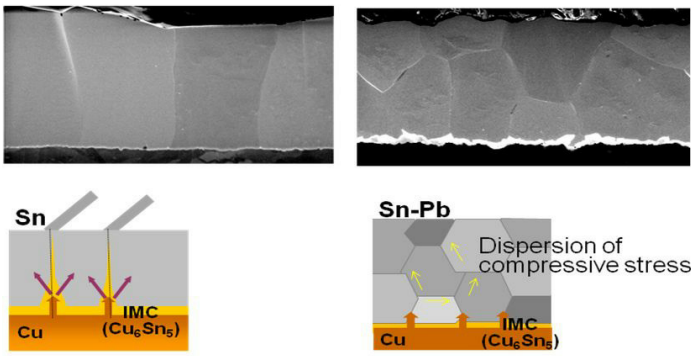


Fig. 12 SEM and schematics of the tin vs tin-lead deposit structures

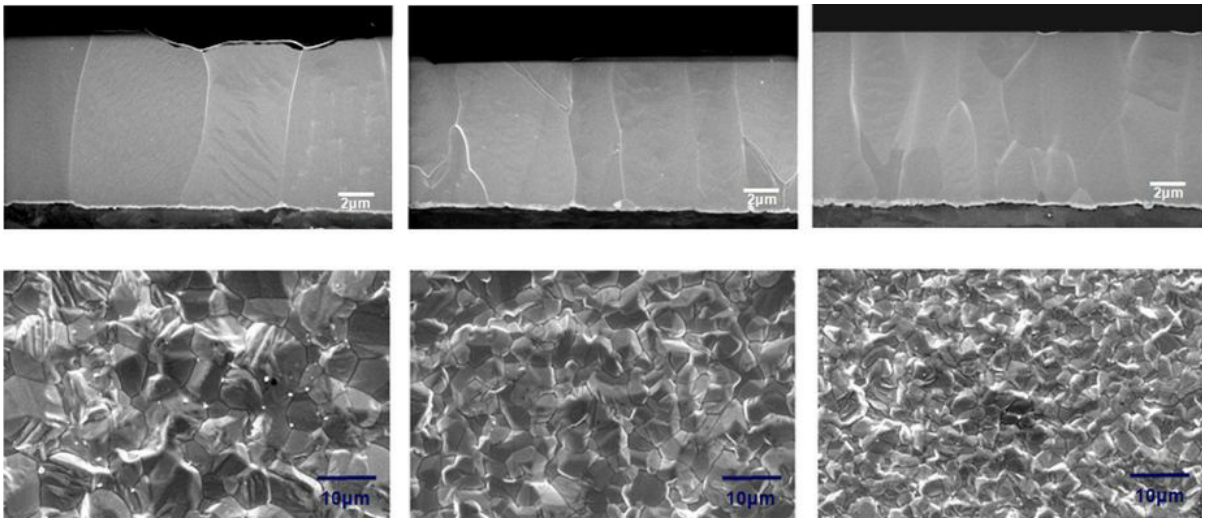
Three types of tin deposits were produced by the use of specific plating additives in the bath:

1) Type "A" was a standard tin deposit characterized by large columnar crystals.

2) Type "B" was modified to produce smaller columnar grain structure.

3) Type "C" was further modified to produce a still smaller grain size that is both columnar as well as equiaxed, almost mimicking the tin-lead structure (Fig. 13).

The levels of the additives in the bath were maintained by continuous dosing. Dosing was based on AmpHrs of plating and results on consistent crystal structure throughout the life of the bath.



Type A *Type B* *Type C*

Fig. 13 shows the SEM of a cross-section and surface morphology of each of the 3 types of tin deposits.

Results and Discussion

All three types were plated to the typical thickness of 10mm (the thickness typical of lead frames) and were placed in an ambient environment (30°C/60%RH) for 4,000 hours.

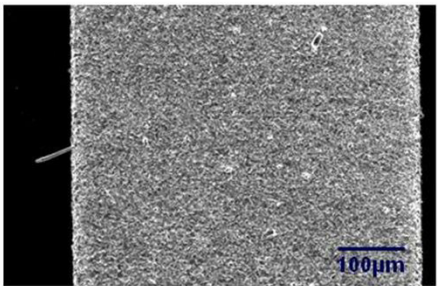


Fig. 14 Type A tin deposit having developed relatively long whiskers

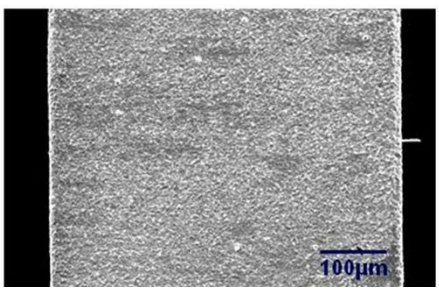


Fig. 15 Type B tin deposit having developed shorter whiskers than Type a

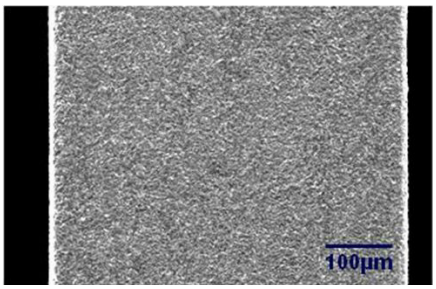


Fig. 16 Type C crystal structure stored under the same conditions. shows no whisker formation

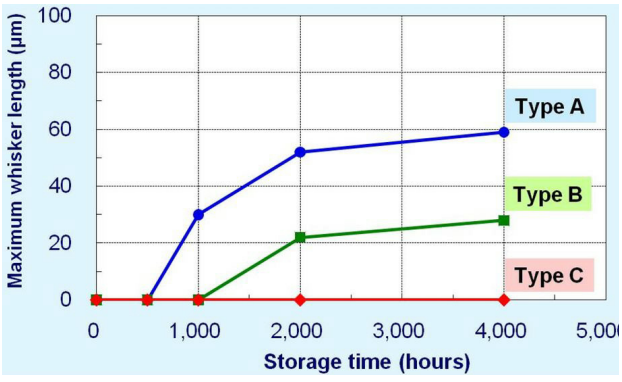


Fig. 17 Graph depicting the length of whiskers vs storage time of the 3 crystal types of tin deposits

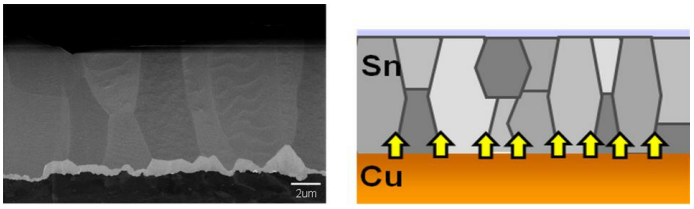


Fig.18 Actual SEM of a cross-section and a graphic presentation of a Type 3 tin deposit.

Fig. 18 is the result of the fine-grained equiaxed crystal structure (type C deposit) achieved by modifying the plating bath with specific types of additives. The result is a very controlled evenly distributed relatively thin IMC, producing minimum stress. The equiaxed crystal structure dissipates the stress resulting in no whisker formation. In this study, no whiskers were observed with fine-grained equiaxed tin deposits stored under ambient conditions for up to 22,000 hours.

Conclusions

In this work two distinct approaches were attempted to restrain whisker growth in tin deposits over copper. The first approach was to create a uniform IMC, by micro-roughening the copper substrate before tin deposition. A uniform IMC would eliminate high stress in localized areas. The second approach was to modify the grain structure, from a large columnar structure to a fine-grained equiaxed structure, resembling that of tin-lead deposit. This was achieved by the use of commercially available, proprietary additives.

Tin deposits which had crystal structures similar to tin-lead deposits restrained tin whisker formation effectively. Crystal structure modification of the tin deposit was thus demonstrated to be a very effective way to restrain tin whisker formation.

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George Milad - Biography

George Milad has over 30 years of experience in PWB manufacturing. He is the National Accounts Manager for Technology at Uyemura International Corporation. Other positions held include Technical Marketing Manager at Rohm and Haas Electronic Materials, Director of Applications at Atotech and Engineering Manager at Automata PWB. He is the author of the chapters on "Plating" and "Surface Finishing" in Clyde Coombs' "Printed Circuit Handbook", Fifth Edition, 2001. George was also the recipient of the IPC 2009 President's award. He presently chairs the Plating Committee and is a permanent member of the Technical Activities Executive Committee of the IPC. George Milad can be contacted at: gmilad@uyemura.com

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Bill Wilkie

The Institute of Circuit Technology

ICT Southern Area Evening Seminar

about

UK PCB Manufacturing in association with the rest of the world

at

17.30 (registration 17.00)

Tuesday 4th September 2012

in the

Newtown House Hotel, Hayling Island

http://www.newtownhouse.co.uk/

Provisional Agenda

Paper from Steve Driver, MD of Spirit Circuits

Paper from Andre Bodegom, of Adeon

Paper from Dr. Pavel Shashkov Director at Cambridge Nanotherm, who will give a presentation on Nano Ceramic Aluminium for LED Thermal Management.

Keynote Speaker will be Nigel Risner, motivational speaker

The four papers will be followed by a Buffet.

This event is Free to members of the ICT and their guests, and is supported by Spirit Circuits

By request, we will issue a 'certificate of attendance', to provide an official record of participation in the event. This certificate can be used to keep professional development records up to date and also as proof of career development.

Register with: **Bill Wilkie**

Technical Director,
Institute of Circuit Technology
Tel - 01573 226 131
bill.wilkie@instCT.org