Standardisation Updates – UL & IEC

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AGENDA

- Dissemination of the standards work
- IEC Standards
  - New Publications of Interest
  - Work in Progress of Interest
- UL
  - Solder limits update
- Summary

DISSEMINATION OF THE STANDARDS WORK

I sit on the following standards committees:

- **UL 796, UL746E, UL 796F, UL 746F**
  - EIPC's representative on the UL Standards Technical Panel for these standards
- **IEC TC 91 – Electronics Assembly Technology**
  - Convenor of Working Group 2 – Requirements for Electronic Assemblies
  - UK Expert on several other Working Groups
- **EPL 501** – UK Mirror Committee to **IEC TC 91 and ISO TC 44 SC 12** (Soldering Materials)
  - Chair of this group; representing ICT
- **IPC 5-32A – Ion Chromatography and Ionic Conductivity Task Group**
  - Vice Chair
- **IPC 5-32C – Bare Board Cleanliness Assessment Task Group**
  - Vice Chair
- Member of several other IPC committees

IEC TC 91 – PUBLICATIONS IN 2019 - SUMMARY

- 9 Publications in 2019
- 5 First Edition Documents / 4 New Editions to Existing Documents (inc. Corr. & Am.)
- 2 Technical Reports / 5 Standards (exc. Corr. & Am.)
- 3 Embedded Component Documents

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC 60068-2-69:2017+AMD1:2019 CSV	Edition 3.1 (this includes the ammendment, also published in 2019)	2019-06-19	Environmental testing - Part 2-69: Tests - Test Te/Tc: Solderability testing of electronic components and printed boards by the wetting balance (force measurement) method
IEC 60068-2-82:2019	Edition 2.0	2019-05-14	Environmental testing - Part 2-82: Tests - Test Xw1: Whisker test methods for components and parts used in electronic assemblies
IEC 61188-6-4:2019	Edition 1.0	2019-05-02	Printed boards and printed board assemblies - Design and use - Part 6-4: Land pattern design - Generic requirements for dimensional drawings of surface mounted components (SMD) from the viewpoint of land pattern design
IEC 62878-1:2019	Edition 1.0	2019-10-14	Device embedding assembly technology - Part 1: Generic specification for device embedded substrates
IEC 62878-2-5:2019	Edition 1.0	2019-09-16	Device embedding assembly technology - Part 2-5: Guidelines - Implementation of a 3D data format for device embedded substrate
Technical Reports			
IEC TR 61189-5-506:2019	Edition 1.0	2019-06-26	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-506: General test methods for materials and assemblies - An intercomparison evaluation to implement the use of fine-pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501
IEC TR 62878-2-7:2019	Edition 1.0	2019-03-20	Device embedding assembly technology - Part 2-7: Guidelines - Accelerated stress testing of passive embedded circuit boards

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC 60068-2-69:2017+AMD1:2019 CSV	Edition 3.1 (this includes the amendment, also published in 2019)	2019-06-19	Environmental testing - Part 2-69: Tests - Test Te/Tc: Solderability testing of electronic components and printed boards by the wetting balance (force measurement) method

This standard outlines the wetting balance method (solder bath and globule) for evaluating both components and PCBs. Covers both Pb and Pb-Free solder alloys.

Significant technical changes since the last edition include:

- Integration of IEC 60068-2-54 (Environmental Testing Part 2-54 Tests Test Ta Solderability Testing Of Electronic Components By The Wetting Balance Method)
- Inclusion of tests of printed boards
- Inclusion of new component types
- Updated test parameters for the whole component list
- Inclusion of a new gauge R & R test protocol to ensure that the respective wetting balance equipment is correctly calibrated

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC 60068-2-82:2019	Edition 2.0	2019-05-14	Environmental testing - Part 2-82: Tests - Test Xw1: Whisker test methods for components and parts used in electronic assemblies

This standards specifies tests for assessing the whiskering propensity of surface finishes of electric or electronic components and mechanical parts such as punched/stamped parts representing the finished stage, with tin or tin-alloy finish.

The test methods have been developed by using a knowledge-based approach.

Significant technical changes since the last edition include:

- Extension of the scope to include electromechanic components and press-fit pins, which are used for assembly and interconnect technology
- Significant reduction of the testing effort by a knowledge-based selection of test conditions i.e. tests not relevant for a given materials system can be omitted
- Harmonization with JESD 201A by omission of severities M, N for temperature cycling tests
- Highly reduced test duration (1 000 h instead of 4 000 h) for damp-heat test by introducing test condition at elevated humidity of 85 % R.H. and a temperature of 85 °C providing increased severity.

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC 61188-6-4:2019	Edition 1.0	2019-05-02	Printed boards and printed board assemblies - Design and use - Part 6-4: Land pattern design - Generic requirements for dimensional drawings of surface mounted components (SMD) from the viewpoint of land pattern design

IEC 61188-6-4:2019 specifies generic requirements for dimensional drawings of SMD from the viewpoint of land pattern design.

The purpose of this document is to prevent land pattern design issues caused by lack of information and/or misuse of the information from SMD outline drawing as well as to improve the utilization of IEC 61188 series.

This document is applicable to the SMD of semiconductor devices and electrical components.

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC 62878-1:2019	Edition 1.0	2019-10-14	Device embedding assembly technology - Part 1: Generic specification for device embedded substrates

IEC 62878-1:2019 specifies the generic requirements and test methods for device-embedded substrates.
The basic test methods for printed board substrate materials and substrates themselves are specified in IEC 61189-3.

This part of IEC 62878 is applicable to device-embedded substrates fabricated by use of organic base material, which includes, for example, active or passive devices, discrete components formed in the fabrication process of electronic printed boards, and sheet-formed components.

The IEC 62878 series applies neither to the re-distribution layer (RDL) nor to electronic modules defined in IEC 62421.

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC 62878-2-5:2019	Edition 1.0	2019-09-16	Device embedding assembly technology - Part 2-5: Guidelines - Implementation of a 3D data format for device embedded substrate

IEC 62878-2-5 specifies requirements based on XML schema that represents a design data format for device embedded substrate, which is a board comprising embedded active and passive devices whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material

This data format is to be used for simulation (e.g. stress, thermal, EMC), tooling, manufacturing, assembly, and inspection requirements. Furthermore, the data format is used for transferring information among printed board designers, printed board simulation engineer, manufacturers, and assemblers

IEC 62878-2-5 applies to substrates using organic material. It neither applies to the re-distribution layer (RDL) nor to the electronic modules defined as M-type business model in IEC 62421.

IEC TC 91 – PUBLICATIONS OF INTEREST IN 2019

Reference	Edition	Date	Title
Standards			
IEC TR 62878-2-7:2019	Edition 1.0	2019-03-20	Device embedding assembly technology - Part 2-7: Guidelines - Accelerated stress testing of passive embedded circuit boards

IEC TR 62878-2-7 describes the accelerated stress testing of passive embedded circuit boards. It can be used for screening finished boards, including multilayer and high-density interconnection (HDI) boards. These boards are mainly for mobile devices.

IEC TC 91 – WORK IN PROGRESS – SUMMARY

- 29 Documents Currently Being Worked On
- 24 New Documents / 5 Documents Being Revised
- 26 Standards / 3 Technical Reports
- 18 Test Methods / 1 Vocabulary / 1 Embedded / 2 Materials for PCBs / 3 Design & Use / 4 Component Requirements

IEC TC 91 – WORK IN PROGRESS – OF INTEREST

Project Reference	Title	Init. Date	Current Stage Date	Current Stage	Next Stage Date	Next Stage
IEC TR 61191-7 ED1	Printed board assemblies - Part 7: **Technical cleanliness** of components and printed board assemblies	2019-05	2020-01	Being Published	2020-02	Published
PNW 91-1638	Thermal resistance test of lamination layer		2020-01	New Work Item Proposal	2020-04	Preparation of results of voting on new work item
IEC 61189-2-803 ED1	Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-803: Test methods for Z-Axis Expansion of base materials and printed board	2018-06	2019-09	Committee Draft to be discussed at next meeting	2020-06	
IEC 61189-2-804 ED1	Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-804: Test methods for time to delamination – T260, T288, T300	2018-06	2019-09	Committee Draft to be discussed at next meeting	2020-06	
IEC 63251 ED1	Test Method for Mechanical Property of Flexible Opto-Electric Circuit Boards under Thermal Stress	2019-05	2019-11	Committee Draft for commenting by NCs	2020-02	Preparation of comments made on Committee Draft document
IEC 61188-6-1 ED1	Circuit boards and circuit board assemblies – Design and use – Part 6-1: Land pattern design - Generic requirements for land pattern on circuit boards	2018-01	2020-01	Translation of Committee Draft for Voting	2020-02	Draft of Committee Draft for Voting circulated to maintenance team

IEC TC 91 – WORK IN PROGRESS – OF INTEREST

Project Reference	Title	Init. Date	Current Stage Date	Current Stage	Next Stage Date	Next Stage
IEC 61188-6-2 ED1	Circuit boards and circuit board assemblies - Design and use - Part 6-2: Land pattern design - Description of land pattern for the most common surface mounted components (SMD)	2019-07	2020-01	Translation of Committee Draft for Voting	2020-02	Draft of Committee Draft for Voting circulated to maintenace team
IEC 61189-5-504 ED1	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-504: General test methods for materials and assemblies - Process ionic contamination testing (PICT)	2017-09	2020-02	Draft circulated of Final Draft International Standard	2020-03	Preperation of report on voting on Final Draft International Standard
IEC 61189-5-601 ED1	Test methods for electrical materials, printed boards and other interconnection structures and assemblies - Part 5-601: General test methods for materials and assemblies - Reflow soldering ability test for solder joint, and reflow heat resistance test for printed boards	2015-11	2019-12	Preparing report on the voting on the Committee Draft for Voting document	2020-02	
PNW 91-1590	MATERIALS FOR PRINTED BOARDS AND OTHER INTERCONNECTING STRUCTURES – Part 6-11: Sectional specification set for reinforcement materials – Specification for finished fabric woven from “Low Dk” glass for printed boards		2019-10	Preparing report on the voting on the New Work Proposal document	2019-11	

IEC TC 91 – WORK IN PROGRESS – OF INTEREST

Project Reference	Title	Init. Date	Current Stage Date	Current Stage	Next Stage Date	Next Stage
IEC 62878-2-601 ED1	Device Embedding assembly technology - Part 2-602: Guideline for stacked electronic module - Evaluation method of inter-module electrical connectivity	2019-04	2019-12	Committee Draft for commenting by NCs	2020-03	Preparing of the compilation of comments on the Committee Draft document

UL – UPCOMING PROPOSALS

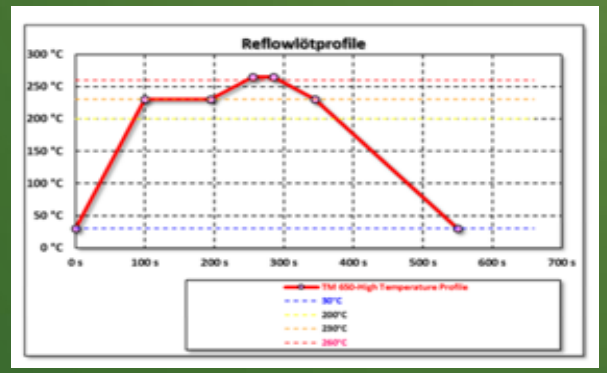
- Solder Limits
  - Been talking about this for several years now
  - Solder Limits are a Recognized parameter for
    - PCBs
    - Solder Resists
    - Metal-Clad Laminates
  - Meant to represent the soldering processes the PCB will be exposed to during the component assembly operations

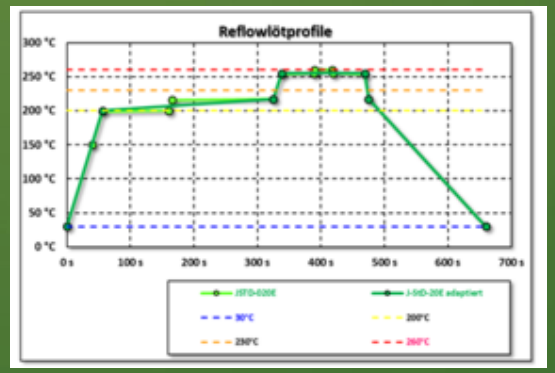
UL SOLDER LIMITS

- Looking to change the term to “Assembly Soldering Process” to provide a better description of what this parameter is
- Default conditions proposed to be 6-cycles of IPC-TM-2.6.27 T260 reflow
  - Could chose alternative conditions of IPC-TM-2.6.27 T245 or T230. Or 6 or 3-cycles.
  - Also possible to use a special reflow profile, if agreed with the OEM/ODM
  - Reflow profile would be considered representative of Wave and Selective Soldering
- The Follow-Up Service Inspectors would be told to check the maximum reflow temperature and the number of soldering cycles that the PCBA is exposed to
  - Will NOT be checking the details of the reflow profile beyond this

UL SOLDER LIMITS

- New limits come after research from FED and ZVEI
- Requested member companies to submit reflow profiles being used
  - Fell within the IPC-TM-650 2.6.27 or J-STD-020E (adapted) reflow profiles





- AT&S conducted testing on 1.6mm and 0.38mm, coated and uncoated, FR-4.0 and FR-4.1, and all samples were able to pass the UL Recognition for Bond Strength & Delamination and Flammability testing

UL SOLDER LIMITS

- No plan to retrospectively apply new Assembly Soldering Process limits to existing board types – would only be new evaluations, once the proposal has been accepted and added to UL 796, UL 746E, UL 796F, and UL 746F
- Still no guarantee that this proposal will be accepted by the UL Standards Technical Panel
- Should know how things will proceed over the coming months
  - The very fastest this could be added to the standards is 6-months, more likely between 8 and 18-months, if accepted

UL – UPCOMING PROPOSALS

- Other corrections / clarifications were proposed during the Standards Technical Panel (STP) meeting but no fundamental changes
- One new proposal was presented at the STP Meeting by the Ventec representative, Alun Morgan
  - Requested the STP to consider moving from using chemistry to define laminate groups, to performance, as this aligns with industry and would help PCB designers in specifying the PCB
  - Initial Task Group will be established to tackle the first step of identifying what each Building Block actually means
    - Currently no definitions for what constitutes a Resin, Secondary Resin 1, Secondary Resin 2, Filler, Flame Retardant, etc.

SUMMARY

- 9 IEC Electronics Assembly Technology publications in 2019
- 29 IEC Electronics Assembly Technology publications at various stages of the standards development process
  - Strongly recommend reviewing the Technical Cleanliness Technical Report!
- UL Solder Limits proposal will see a default set of conditions of 6x T260 reflow profile used
  - But still a proposal, so nothing is certain yet

CONTACT DETAILS

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