Journal of the Institute of Circuit Technology

2007 Events

6th February	Council Meeting Evening Seminar - Leeds
2nd / 5th April	Annual Foundation Course at Loughborough University
3rd June	Evening Seminar at Arundel supported by Artetch Circuits
21st August	12.30 Council Meeting - London Canal Museum
20th September	33rd Annual Symposium at NPL
10/12th October	*EIPC Copenhagen, Clarion Hotel*
31st October	17.30 Evening Seminar, Pike & Eel Hotel, St.Ives, Cambridgeshire. supported by Anglia Circuits
4th December	14.00 Council Meeting 17.30 Evening Seminar, White Swan Hotel, Arundel. - Design for Manufacture . supported by Artetch Circuits

2008 Events

24/25th January	*E IPC Winter Conference, Rome*
12th February	14.00 Council Meeting 17.00 AGM 17.30 Evening Seminar, all at White Swan Hotel, Arundel.
4th March	17.00 Evening Seminar, Davenport, Hotel, Darlington
16/22nd March	*6th EIPC Technology Trip Shanghai, China*
31st April	Annual Foundation Course at Loughborough University
3rd June	34th Annual Symposium, at Tweed Horizon Centre, Newtown, St.Boswells
5th August	15.00 Afternoon Seminar, in Design Suite, Loughborough University

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Editorial

Welcome to this new Initiative by the Institute, our first official *Journal.* The contents will be varied from News Items, Seminar and Symposium Reports, Technical Articles and many other features. Initially the *Journal* will be published quarterly in a format for circulation to Members electronically.

The success of the *Journal* will, however, depend upon receiving material for publication and Members are encouraged to participate by submitting Items for inclusion in the *Journal* such as News Releases, Technical Articles and similar which will be of interest to other Members..

The Institute of Circuit Technology is now in its 33rd year, having been formed in 1974. Much has changed over this period, both technically and commercially. The objectives of the ICT are to represent the Printed Circuit Industry from a technical and productivity point of view whereas there are other august bodies dedicated to its commercial aspects.

Our current activities include Foundation Courses in Circuit Manufacture, Master Classes in specific subjects, regular Evening Seminars held in various parts of the Country and full scale One Day Symposia. We also have an active Web Site http://www.instct.org open to all with a Forum dedicated only to Members, into which they can make contributions.

You may know Colleagues who are not yet Members of the Institute and you are encouraged to lobby them to join, for the more Members we have the more our position is strengthened, which in turn allows us to broaden our Activities.

A recent innovation is the establishment of "Group Membership", a special arrangement where for a fixed annual fee, Organizations can enrol a limited number of named staff en bloc . Full details can be obtained from Bill Wilkie**.**

Please support the *Journal,* send contributions to Bruce Routledge. All addresses can be found on the Web Site.

John B. Walker Hon. Sec.ICT

Membership

New members voted into membership by the Council 21st August 2007

Associate Members (A.Inst.C.T.)

Jason Clewes	10034	Chaya Losada	10041
Mark Hasdell	10036	Peter Watson	10042
Paul Bennett	10037	Peter Turbull	10043
Andrew Odell	10038	Cyril Stockhill	10044
Mike Normansell	10039	Douglas Gallagher	10045
Barry Hough	10040	John Chappell	10046
		Leslie Blakeham	10049

Members (M.Inst.C.T.)

James Pearson	10047	Ian Johnson	10054
Nigel Stone	10048	Steve Hirst	10055
Richard Ross	10050	Stuart Cunningham	10057
Tony Teasdale	10051	Chris Williams	10058
Mark Goodwin	10053	John Cornforth	10059

Fellows (F.Inst.C.T.)

Mike Osmond	10052	Paul Watson	10060
Walt Custer	10056	Alex Ross	10061

Regrading to Fellow (F.Inst.C.T.)

Steve Kerr 10021

Honorary Fellow (Hon.F.Inst.C.T.)

Ronald A Neale 5

(Mr Neale - as far as we are aware - is the last surviving member of the first Council formed by the Association of Printed Circuits , the body from which the Institute developed. He continued to serve on the ICT Council for many years.)

Technical News

NPL National Physical Laboratory Industry Defect Database

NPL Electronics Interconnect Team is creating a defect database as part of their continuing support to the electronics industry available at http://defectsdatabase.npl.co.uk There is a strong belief that many of the component, printed circuit board, assembly and solder joint failures are often common to many parts of the industry worldwide. By collecting together common problems and making example images available it will assist engineers implement corrective actions in their process or design. It will also pinpoint common trends to guide the NPL team in correctly identifying future projects to maximise its benefit to industry.

The database was suggested as an industry project by two members of the Industry Advisory Group IAG, recommending that NPL were best equipped to coordinate the activity due to their scientific and manufacturing expertise. To achieve this NPL aim to create an online database of problems provided by the industry in a confidential manner. The process problems and most common solutions will be available via the Electronics Interconnection web page and be freely accessible.

The aim of the database is to include the following information in an interactive searchable database:

Example defects or failures
Material type
Probable causes
Product application and service environment
Product volume
Percentage failure

It is possible to create a useful reference source but still provides a confidentiality of the actual product or company involved. You can email your production problem images or request support from davide.di.maio@npl.co.uk

To further assist and aid a better understanding of industry problems from a supplier's prospective NPL will be circulating three surveys to establish the most common problems experienced. The short surveys are aimed at:

Printed Circuit Board Manufacturers http://defectsdatabase.npl.co.uk/surveys/pcb.pdf
Component Manufactures/Distributors
http://defectsdatabase.npl.co.uk/surveys/components.pdf
Printed Board Assemblers http://defectsdatabase.npl.co.uk/surveys/assembly.pdf

Often suppliers to the industry are faced with potential problems from their customers and by comparing survey results and actual defects submitted to NPL will allow a better understanding of common problems and their relative frequency.

Bob Willis

ICT Annual Symposium 2007

The 33rd Annual Symposium of the Institute of Circuit Technology was held on 20th September 2007 at the National Physical Laboratory. ICT Technical Director **Bill Wilkie** welcomed delegates, commenting that the membership list continued to grow and that the increasing proportion of younger members was an encouraging trend for the future.

Dr Chris Hunt began the proceedings with an update on current NPL projects, particularly relevant being the compilation by the Electronics Interconnection Group of an online Defects Database, the objective being to make defect information available to assist engineers to implement corrective actions in their process or design. He invited delegates to contribute to the survey, making it clear that examples would be presented in an anonymous format for the benefit of the industry as a whole.

The keynote paper, on Future Trends in Interconnection Technology, was given by **Professor Martin Goosey**, Industrial Director of the Innovative Electronics Manufacturing Research Centre based at University of Loughborough. Thirty projects were currently being coordinated by IEMRC, many of which related to advanced interconnection device technologies. Moore's Law still continued to hold, the number of transistors on a chip doubling every two years, and it was projected that by 2010 devices working at 10GHz with billions of transistors would be available. Packaging was evolving into a nano-scale of dimensions, and the System-in-Package concept was becoming mainstream technology. Challenges for the printed circuit industry were not only in the provision of interconnection solutions for increasingly complex devices and packages, but also in environmental compliance. Possible directions included buried components, both passive and active, and embedded waveguides. The integrated optical and electrical interconnected printed circuit board, designated OPCB, was a major area of interest within IEMRC with work proceeding on the development of design rules and cost-effective production methods. From an environmental perspective, sonochemical techniques offered ways of preparing surfaces for metallisation using acoustic cavitation rather than aggressive chemistry. IEMRC's future programme included the evaluation of carbon nanotubes as means of creating nanoconnections and making optically transparent conductors.

Karl Miles of Goepel Electronic gave an insight into the testing of devices and assemblies by boundary-scan techniques. Boundary scan testing was developed as the JTAG (Joint Test Action Group) interface to solve physical access problems on increasingly crowded assemblies, using test circuitry embedded at chip level, and could be used to access even the most complex assemblies for testing, debugging and in-system device programming and for diagnosing hardware problems. The need for physical test points on the board was eliminated or greatly reduced, leading to savings as a result of simpler board layouts, less costly test fixtures and reduced time on in-circuit test systems. Access to the electronics was via a standardised 4-wire or 5-wire serial interface, allowing test clock, test mode select and test data input signals to be connected whilst test data output was collected. The technique was also very effective for HALT, HASS and ESS testing because the simple interface enabled straightforward connection to an assembly within an environmental chamber.

Martyn Gaudion of Polar Instruments explained with very clear illustrations how loss is becoming a key parameter which PCB designers need to understand. Until recently, the main area of concern with transmission lines had been reflection, but for the future the management of the "loss budget" would become increasingly important. As frequencies increased, loss occurred progressively in both copper and dielectric. In a copper conductor, a high frequency signal was effectively carried not in the bulk material, but in its surface layer, as a "skin effect". As conductor geometries became finer, the skin effect became more pronounced and surface roughness, such as produced by bonding treatment during laminate manufacture, contributed increasingly to signal loss. Dielectric loss was convincingly demonstrated by observing how FR4 material could be very easily heated-up in a microwave oven, whereas low-loss materials stayed cool in similar conditions. Several routes were open to the designer to reduce loss, but generally resulted in increased cost, and there was a strong case for better communication between designer and fabricator. Tools were becoming available for predicting loss, and an IPC committee was working on the development of standardised test methods.

Dennis Price of Merlin Circuits reviewed trends in flex-rigid PCB manufacture. Whereas flex-rigids had traditionally been too expensive to use for other than mission-critical and aerospace products, they were now finding increasing application in computers and mobile phones, and substantial growth was forecast in automotive, industrial and consumer sectors. BPA figures indicated that the world market for flexible circuits was US$ 7.8 Bn in 2006, of which 7.3% was flex-rigid, and would grow to US$ 11.2 Bn by 2012. Low-cost flex-rigid constructions had been developed which avoided

the need for expensive polyimide materials by using depth-routed FR4 with flexible solder mask in the bend area. Circuits of this type could be processed through normal rigid-multilayer production facilities with standard desmear processes. Alternatively a wide range of semi-flexible core materials was available where tighter bend-radii were required. A novel low-cost construction, developed by Ruwel using copper foil selectively coated with a flexible polymer as the precursor of the bend area, offered extremely good dynamic flexibility at bend radius as small as 1mm.

Bob Willis recounted some experiences of the assembly of flexible circuits using lead-free soldering processes, both convection and vapour-phase. He stressed the importance of good pallet design and highlighted many practical details, particularly the significance of thermal mass, proper support of the circuit whilst avoiding stress or distortion, and the provision of effective drainage for vapour-phase fluid. He discussed aspects of stencil design, choice of solder paste, printing parameters, component placement and the thermal profiling of convection and vapour phase systems, then showed the results of live experiments which had been conducted at Nepcon and Productronica workshops. He described a simple in-process test for wettability which could easily be incorporated into the design of every assembly, consisting of a pattern of dummy conductor strips upon which were printed dots of solder paste at decreasing spacing. Observing to what extent the dots coalesced during reflow gave a meaningful indication of wettabilty of the solderable finish.

Len Pillinger, Certification Manager for BSI Product Services, reviewed the evolution and obsolescence of traditional capability approvals, and explored ways in which BSI could provide certification relevant to the future needs of the industry. He reported the results of a survey conducted to determine the awareness of the UK printed circuit industry to the IPC standards IPC-A-600G and the IPC-6011 series, A-600 being a basic workmanship standard and the 6011 series being analogous to MIL spec, more rigorous than previous BS/CECC standards. The survey indicated a polarisation of the industry, with the high-reliability market at one extreme and the commercial market at the other, and little in-between. There was a general awareness of IPC-A-600 across the industry both by fabricators and their customers, but less for IPC-6011, and it was clear that different levels of certification were required to satisfy the needs of different market sectors. BSI proposed two separate approvals, a "kitemark" system based on IPC-A-600 for commercial applications and an IEC/IECQ-CECC system based on IPC-6011 for high-reliability applications, and it was expected that these would be generated during the coming year.

Mike Inman, Scheme Manager from BSI Product Services, gave an introductory overview of the onerous implications for the electronics industry of European Union REACh legislation. REACh was a "regulation" rather than a "directive", meaning that it became law as soon as it was implemented in June 2007, and its stated objectives were to achieve better human health, a cleaner environment and a more sustainable European chemical industry. The regulation replaced 42 pieces of existing legislation, whilst citing many other directives and legislation, and was estimated to apply to 100,000 "substances", each of which would eventually have to be registered, evaluated and authorised. Companies would have to provide information on all substances they wished to produce or import in quantities of at least 1 tonne per year. This information would be stored in a central database managed by a European Chemicals Agency based in Finland, and data not covered by industrial confidentiality would be accessible to the public and downstream users. This data would include the toxicological and ecotoxicological properties of the substance, proposals for labelling, instructions for use, etc. Given the large number of existing substances, registration would be performed in tiers over a period of 11 years. Substances of high tonnage, and substances of very high toxicity, would necessitate the most data and would be registered first. BSI could offer guidance and training in developing REACh strategies.

Continuing on the theme of EU legislation, this time with reference to the WEEE directive, **Martin Wickham** from National Physical laboratory reported progress of a project to determine the practicability of unreinforced thermoplastics as printed circuit substrates, with re-usability and recyclability of materials as the objective. An estimated 85% of PCB scrap currently went to landfill, because once metals had been recovered, little could be done to salvage anything useful from reinforced thermoset laminates. Polyetherimide, as used in the production of moulded circuits, had been used as substrate for the trials, although several other thermoplastic materials were available. Panels had been drilled, electroless plated, electroplated, imaged, etched and finished as printed circuit boards. Because of the sensitivity of polyetherimide to soldering temperatures, conductive adhesives had been used for assembly and low-resistance joints had been achieved. Test assemblies had shown low levels of failure on thermal cycling, the resilience of the conductive adhesive compensating for the thermal expansion mismatch between substrate and components. Encouraging results had also been observed on assemblies built with a low-melting tin-bismuth solder. Much work remained to be done on establishing procedures and infrastructure for recycling the thermoplastic material, and the project was ongoing.

The 33rd ICT Annual Symposium provided not only a forum for the dissemination of knowledge of printed circuit and related technologies, but also a busy table-top exhibition area and excellent opportunities for delegates to network with their peers. A very successful event: Bill Wilkie thanked delegates for their attention and exhibitors for their support, and acknowledged the cooperation of National Physical Laboratory in providing a superb venue and facilities.

Pete Starkey
ICT Council
September 2007

Towards Greener Printed Circuit Board Production

Martin Goosey

IeMRC Industrial Director
Wolfson School of Mechanical and Manufacturing Engineering
Loughborough University
England

Introduction

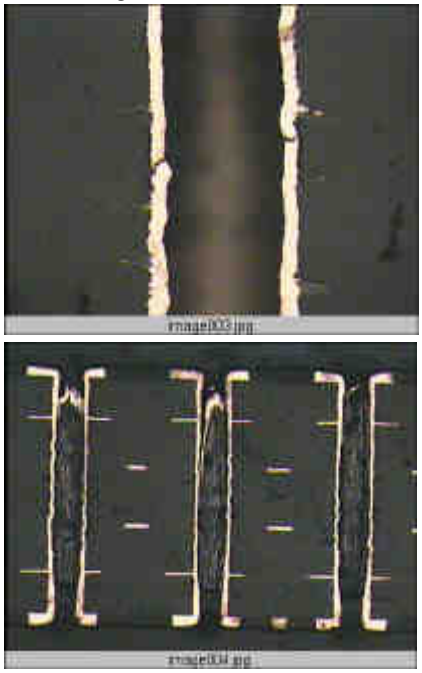
There is a growing awareness of the need for industry to operate in a more sustainable manner and to minimise its impacts both on people and the environment. This is particularly true in the Printed Circuit Board (PCB) sector, where some of the materials traditionally utilised in PCB manufacturing are increasingly deemed to be undesirable and where legislation is now influencing their continued use. Coupled with limitations on the use of specific materials, there is also pressure for the industry to generate less waste from the manufacturing processes it uses and for it to recover and recycle materials when ever possible.

The move to lead-free assembly has, for example, not only required changes in the solders that are used; it has also brought about changes in PCB materials and processes. There is now a much wider range of materials and process and it is important that the correct choices are made if environmental compliance is to be achieved without compromising yields and assembled board reliability.

Implications for PCB Materials

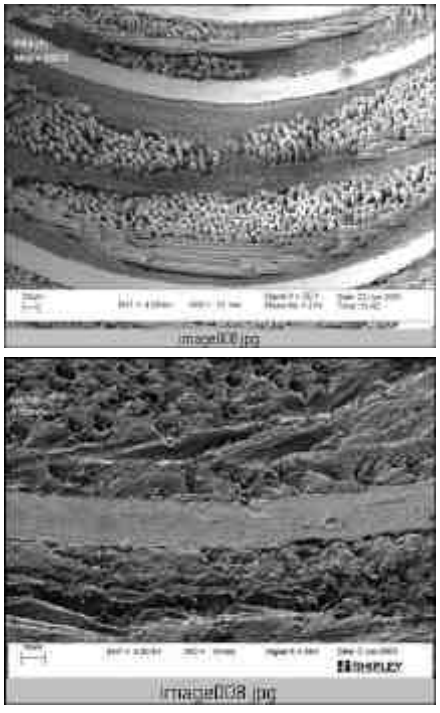
Although the PCB manufacturing industry may not have been affected as much as some of the other parts of the electronics industry supply chain in terms of the number of materials that are restricted or have to be replaced, the new and emerging legislation has placed significant demands on both laminate suppliers and those manufacturing circuit boards. Firstly, and perhaps most importantly, the move to lead-free assembly has meant that assemblers are now using alloys with melting temperatures that are higher than those of the traditional tin-lead alloys. There has already been a huge amount of research work undertaken to identify and address the many potential problems that can arise when converting to lead-free assembly and a discussion of these is beyond the scope of this short paper. However, the move to higher soldering temperatures may also have significant implications for the choice of laminates that are used for a particular board type. While many of the more ominous predictions about the influence of these higher temperatures and new solders have turned out to be less serious than initially predicted, it is still true to say that the one of the biggest concerns about converting to lead-free assembly is focused on the effects of higher soldering temperatures on laminate materials and subsequent assembled board yields and reliability.

An important issue for PCB fabricators is to ensure that the laminate materials used are able to survive the elevated soldering temperatures common with lead-free assembly. This can be a particular problem for large, thick boards heavily populated with many components and which need several solder cycles. As a general rule, the better the quality of laminate used, the more likely it is to be able to survive multiple lead-free solder cycles. One of the problems associated with lead-free assembly is caused by the additional z-axis expansion during excursions to higher soldering temperatures. This can cause issues with plated through hole reliability via barrel cracking and related issues.



Barrel cracking in a 6 layer 'higher Tg' FR4 board exposed to lead-free assembly conditions

One way of reducing these stress related effects is to reduce the overall thermal expansion, and hence expansion mismatch between the laminate and the copper barrel, by selecting laminates with higher glass transition temperatures. However, whilst this approach can undoubtedly help, there are always other trade-offs and factors that need to be taken into account. Consequently, laminate manufacturers have developed new materials that reduce the likelihood of these types of problems occurring and a wide range of lead-free compatible laminates is now available. For example, laminates containing new curing agents, such as those based on the use of novolac resins have been introduced, as have laminates that contain particulate fillers. While these new laminate materials are designed for use with lead-free assembly, it is important to understand that they may require changes to be made in the metallisation processes used to produce plated through holes. For example, because of their higher crosslink densities and hence more robust chemical structures, modifications to the desmear and hole wall texturing processes may be required in order to give good PTH reliability.



The different textured structures of drilled holes in conventional FR4 (top) and a higher Tg material (bottm)

Although traditionally flame retarded laminates such as FR4, which use brominated resins based on tetrabromobi-

sphenol A, are not affected by the RoHS Directive, there is a growing reluctance to use halogenated materials and a desire in many areas to become halogen-free and thus bromine-free. This move has been driven by concerns over the persistence of bromine containing species in the environment and their ability to cause health problems. Laminate manufacturers have thus been developing alternative halogen-free laminates and numerous materials are now commercially available. These use new classes of flame retardants such as those based on phosphorus. Again, these changes to the basic composition of the laminates can have implications that must be taken into account. Interestingly, and perhaps not surprisingly, changing the curing agents and flame retardant systems has an impact on the thermal stability of laminate materials. Replacing dicyandiamide (DICY) with a phenolic eg novolac material leads to differences in the crosslinked structure of the cured resin and thus its subsequent performance. Similarly, changing the flame retardant can have an impact and replacing brominated resins with new systems has, for example, been reported as offering improvements in thermal stability.

One other area where there could be issues for PCB fabricators is in the inadvertent inclusion of proscribed materials in metals deposited from plating solutions during the board manufacturing process. Metals such as lead and mercury have sometimes been used as stabilizers for plating chemistries and, although they are typically used at very low levels, concerns have been raised that, under certain conditions, it may be possible for these stabilizers to be co-deposited in metal films at levels that could exceed the Maximum Concentration Value allowed by the RoHS Directive.

With the move to lead-free, it will no longer be possible to use the popular tin-lead HASL finish on circuit boards. Fortunately, with the move over the last twenty years or so to increasingly smaller surface mount devices and fine pitch assembly, several planar solderable finishes have been adopted for widespread use. Examples of the most popular ones include immersion tin, nickel-gold, organic solderability preservative (OSP) and immersion silver. Each of these is well established but it should be noted that they can all exhibit problems in some circumstances that could compromise their overall performance. For example, there are concerns about tin whisker formation with some immersion tin processes since this can cause latent reliability problems. Also, the tin deposition process can employ thiourea, which is increasingly unpopular. Similarly, nickel-gold finishes, whilst giving excellent solderability, can suffer from a problem known as black pad that causes in-service reliability issues. OSPs offer a very simple and attractive alternative to tin-lead HASL but, depending on their chemical composition, they may not be able to survive multiple solder cycles without exhibiting reduced solderability. OSPs have also been found to exhibit inferior wetting performance with lead-free solders. Although the above issues can cause problems, these materials can and do provide a good range of viable alternatives to traditional tin-lead HASL finishes, as long as they are used in the recommended way and that their limitations are understood. In recent years, the suppliers of these processes have improved the performance of their products they are often now much improved.

Summary and Conclusions

The PCB industry plays a vital role in a global electronics industry that is increasingly being driven by both consumer pressure and legislation to behave in a more sustainable and environmentally friendly manner; electronics now have to be seen to be green. In recent years PCB manufacturers have been particularly impacted by legislation such as the RoHS Directive and the general move to lead-free assembly. This has caused them to modify their manufacturing processes and suppliers to offer new materials with enhanced performance. It is important to understand the implications of changing these materials and processes, if reliable boards are to be produced. The industry also uses a wide range of chemicals in its manufacturing processes and these can lead to the generation of large quantities of effluent. This effluent contains potentially harmful materials that could damage the environment if not properly discharged and which are increasingly expensive to waste treat. The PCB industry is also under pressure to reduce its costs, to recycle and reuse materials and generally to behave in a more sustainable ands environmentally friendly manner: new technologies that can help reduce costs by enhancing the efficiency of PCB manufacturing are thus to be welcomed. In summary, the pressure on the PCB industry to move towards more sustainable and green processes has resulted in the development of new materials and manufacturing processes that allow circuit boards to be produced with less use of hazardous materials and the generation of less waste, while still enabling the electronics industry to continue its inexorable progress towards ever more sophisticated and technologically accomplished products. Long may this progress continue.

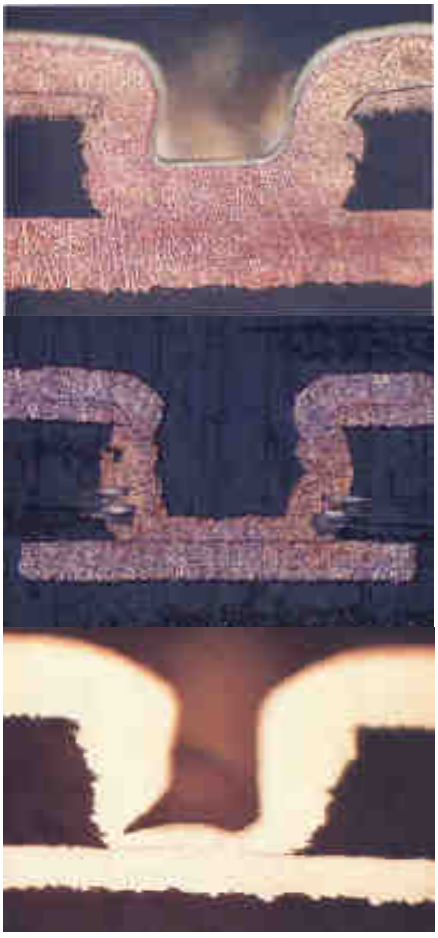
Assessment of Blind Via Holes – An Alternative Approach

Bob Willis - ASKbobwillis.com

(Quote Line)
"Simple and easy way of assessment of blind vias, making failure analysis easier to perform and producing less controversy".

It has become common practice to use blind vias in many portable electronics products. Experience has shown that this method of interconnection is reliable provided the fabrication process is well defined and controlled. Both through hole, blind and buried vias can stand-up to conventional and lead-free manufacture as the length of the barrel is fairly short. It is, however, still difficult to inspect via locations during the fabrication process and there is often great debate on the cause of any failure or if a particular via is satisfactory of not.

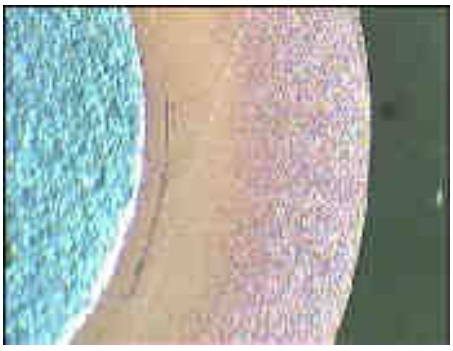
The following images show typical examples of different via connections.



It was a little unfortunate that the IPC-A-600G did not address the issue of via assessment when it was last updated and released during 2004. It is hoped that this will be addressed during any future planed revisions. Blind and buried vias have been used in the industry for many years. Great experience exists, but very few standards or inspection guidelines exist for a company to reference. Producing a microsection is still the most common method of via assessment. Engineers who have learned the procedures of microsectioning will state that it requires great level of skill and experience to correctly prepare and make assessment of a blind via. Often the assessment can be debated due to the methods of sectioning and the final etching process used on the copper layers.

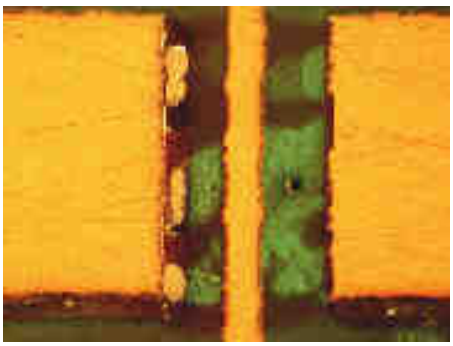
Recently Interconnection Stress Test (IST) has been used by companies as an assessment tool to examine the reliability under simulated operational conditions. A test coupon is designed to simulate the via pattern based on the design rules used on a product family. The test coupon features a heating circuit which allows a DC current to pass through internal layers to simulate the operating conditions of the PCB. This stresses the vias and by monitoring the changes in resistance can determine the expected life of the product based on design rules, manufacture standard and quality of the process. Although the testing and reliability of a particular set of coupons can be determined, final assessment of the failure mode requires a microsection. Further details on IST can be obtained from www.pwbcorp.com

Over the last year experience has been gained in using a different approach, or perhaps just coming at the problem from a different angle. Over many years engineers have produced traditional microsections looking at plated through holes along the length of the barrel. In the case of multilayer boards if any concerns were seen on barrel plating and inner foil separation experienced engineers would turn the section around and examine the copper pad connection.



The images above show a traditional section and copper foil separation. The second image shows the copper pad and the inner copper barrel separated, the third image is at a higher magnification.

This is achieved by grinding the section up through the barrel and illustrates if complete or only partial separation is



Back grinding of section has also been used on board assemblies to look at voiding, solder shorts and corrosion under chip components. The example shows solder shorting and voiding under the chip component when viewed from under the pads.

Examination of Blind Vias by Back Grinding

The following procedure may be used to examine blind via hole interconnections for routine testing or during failure analysis of a printed circuit board. The illustrations outline the typical procedure and the information that may be obtained from any via.

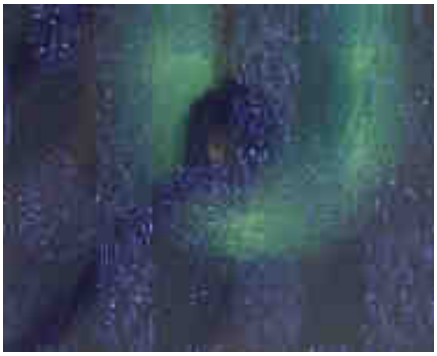
Cut a section of the board containing the via or group of via holes under examination. This can be conducted with a rotary saw to minimise damage to the board or flexing thin substrates. Examination of the Gerber files can help to determine the points of interest provided the fault location have been determined by electrical test. The design files can also show other via positions in this particular layer.

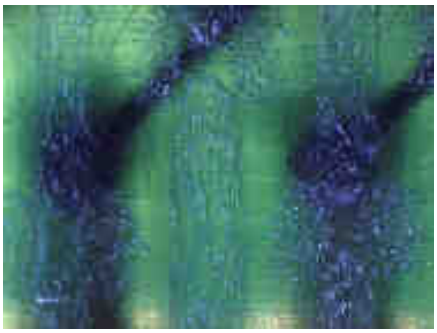
Clean the board section in IPA to remove any surface contamination. This also ensures the mounting resin will

adhere correctly during curing. Mark the section of the board or make up a reference diagram/photograph so the correct via or vias are being examined at all times.

Place the board section in a micro-section mould. The section of the board is placed in the mould so the back of the via or capture pad is facing down. Slowly pore the epoxy mix to cover and surround the section of the circuit board. The epoxy is simply being used to hold the board during the grinding operation.

Place the section mould in an air circulated oven and allow the epoxy to cure. When the epoxy is fully cured carefully remove it from the mould and start grinding the exposed face of the board towards the back of the via hole capture pad. Grinding can be conducted initially using a 400 grit then reducing to a 600, 800 grit paper to slow down the epoxy removal rate. Scratches are not really an issue in this procedure but control of the depth is more important.





Example via and track patterns visible through the PCB during grinding

Check the depth of grinding regularly with a microscope or 20x eye glass to check when you are approaching the pad surface. Ideally you are trying to reach the base copper foil surface or the epoxy layer just below the copper track and pad. With care, and keeping the section flat, you should be able to examine more than one via interconnection using this technique. If more than one via can be examined then a better understanding of the quality of the interconnection can be made. If this technique is only being used for failure analysis of a specific via other vias can be examined first without disturbing the via in question. They allow an engineer unfamiliar with the technique to practice.

The images shows tracks leading to the blind via 0.020" capture pads and close up of pad just below the copper foil

Image of one track cut in preparation to via pad removal and the second prior to cutting the track between via pad and through hole via

When you have ground the section to the base of the copper foil place it under a microscope and probe the track end connected to the capture pad then peel the track from the surface of the epoxy. If during grinding you do reach the copper surface you will put far less strain on the track and copper pad during peeling. When you peel back the copper track you will also separate the capture pad from the base of the plated via.

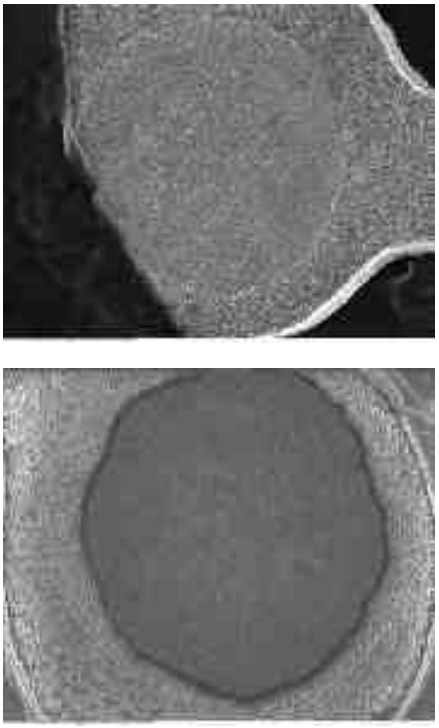
Close up of blind via pad after removal, the surface of the copper under the via hole and close up of copper surface which is approximately 0.010"

Place the track and connected pad in a sealed container for future examination, also place the section in another sealed container. Correct storage of the samples prevents any debris falling on the two surfaces and possibly confusing any future analysis.

Both of the mating surfaces of the blind via that have been separated can be carefully examined. First examination is conducted with a high magnification microscope to look at the previously

mating surfaces. It should be possible to compare the surface of each and show how they have separated, if the copper plating to the pad was defective or not. The two surfaces should have features that match like two jigsaw pieces. When a via is filled with solder during reflow and the copper wall plating is thin you will see the copper barrel and solder separation.

Using an SEM images can be taken of both mating surfaces, a mechanical break between two copper surfaces should provide a distinctive pattern allowing comparison on both surfaces. If the vias were correctly formed with a sound metallurgical bond but failed due to assembly or rework conditions a hard fracture would be noted.



The two SEM images above show the surface of the 0.020" 0.5mm capture pad after separation from the bottom of the 0.010" 0.25mm blind via.

There is no evidence of a fractured surface suggesting that a true bond could not have formed during the blind via plating process. Although no measurement of the force to remove the capture pad has been made, the bond was noticeably weaker that pads of the same size on known good vias.

If the quality of the plating, hole and pad surface preparation was poor then surface analysis on an SEM should be able to identify and characterise any contamination. It could then compare with the surrounding materials used in the fabrication process.

This method of via assessment can be an alternative method of assessment. Gaining practical experience in its use will depend on experience and the number of different failure modes that can be examined.

Bob Willis is a process engineering consultant and one of the most well known providers in the industry of theory and hands on training courses. Bob will be presenting seminars at Productronica, Germany on lead-free inspection and quality control and printed board design for lead-free. Bob has also produced a comprehensive range of interactive training CD-ROM on electronic manufacture. He may be contacted at www.ASKbobwillis.com

Edited and electronically compiled by Bruce Routledge on behalf of the Institute of Circuit Technology.
c/o 30 New Road, Penn. High Wycombe, Buckinghamshire, HP10 8DL