Journal of the

Institute of Circuit Technology

2008 Events

24/25th January	*EIPC Winter Conference,Rome*
6/7th February	*Southern Manufacturing & Electronics FIVE, Farnborough, Hants*
12th February	14.00 Council Meeting 17.00 AGM 17.30 Evening Seminar, all at White Swan Hotel, Arundel. Supported by Eurotech Group plc
4th March	17.00 Evening Seminar, Davenport Hotel, Darlington.
16/22nd March	*6th EIPC Technology Trip, Shanghai, China.*
18/19th March	*Midlands Manufacturing Technology 08 Exhibition, Ricoh Arena, Coventry*
31st March / 3rd April	Annual Foundation Course, Loughborough University.
22nd May	12.30 Council Meeting - London Canal Museum
29/30 May	*EIPC Summer Conference Dresden*
3rd June	34th Annual Symposium, Tweed Horizon Centre, Newtown, St.Boswells.
3rd July	*PCB Inspection & Quality Assessment – Practical Solutions - St Albans askbobwillis.com*
4th July	*IeMRC Annual Conference - Loughborough*
10th July	11.30 One Day Symposium, The Mead Inn, Denmead, nr Waterlooville, Hampshire. Supported by Cookson Group.
5th August	15.00 Afternoon Seminar, Design Suite, Loughborough University.
September	17.00 Evening Seminar, Davenport Hotel, Darlington.
October	Evening Seminar, Exeter
December	17.00 Evening Seminar, Comfort Inn, Arundel.

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vol.1 no.3 June 2008

Editorial

Our third edition, and the first to have an Editorial from the editor. My colleagues John Walker - *Secretary* , and Steve Payne - *Chairman* have given you a very clear picture of The Institute of Circuit Technology's objectives and past achievements, so it would be appropriate to introduce a little controversy.

The article "Tin Whiskers" which is reproduced from 'the**guardian**Thursday 03.04.08' - 'technologyguardian' section is a report by **Kurt Jacobsen** of a peculiar phenomenon first learnt about at a lecture organised by the Institute of Metal Finishing at Borough Polytechnic about 45 years ago, when it was alleged to have caused a fault in Post Office telephone relays. The interest at that time was the production engineering aspect of 'Anita' - the 1st electronic calculating machine at the Bell Punch Co. in Uxbridge. The problem was bypassed by using palladium plated switch contacts instead of tin plated.

Mr Jacobsen reports about numerous serious failures alleged to have been caused by whiskers, since that time. This was during the period when tin/lead alloys were commonly used, now without lead to 'tame' it, can we expect more failures ?

Your experiences please, in letters or e-mails to the *Journal.*

At the time of an Institute of Circuit Technology Symposium held in Edinburgh some 25 years ago the subject of "Optical and Electronic Interconnect" was discussed and Edinburgh University was mentioned as where research was in progress. Also at that Symposium the Plessey Co. had a comprehensive paper on Surface Mount - the only snag being the unavailability of suitable components !

Meetings of Institutes bring large numbers and kinds of problems and solutions to the fore - the individual's problem is to sort out the wheat from the chaff.

Your letters could help you and your colleagues.

Bruce Routledge

Membership

New members voted into membership by the Council 22nd May 2008

Associate Member (A.Inst.C.T.)

Zoe Kolleng	10086
Christopher Bond	10093
Greg Jackson	10097
Paul Worth	10098
Mike Smith	10099
Jason Benning	10100
Jason Hassell	10101
Don McEwen	10102
Andy Hobbis	10103
Jonathan Cohen	10104
Tod Thornber	10105
Agnieska Wozna	10106
Karen Hughes	10107
Stephen Wallace	10108
Craig McDonald	10109
Martin Knight	10110
Oscar Fernandez	10111

Members (M.Inst.C.T.)

Mark Loader	10082
David Wood	10083
Paul Crier	10084
Iain Hirst	10085
Patricia Moss	10087
Robert Hopkins	10088
Darren Watson	10089
Craig Soley	10090
Joolz Burt	10091
Matthew Beadel	10092
Matthew Kember	10094
Jeremy Rygate	10096
Sue Critcher	10112
Mike French	10113
Alan Broomfield	10114

Fellow (F.Inst.C.T.)

Brian Shorrock	10095

Corrections and Clarifications

The **Council Members 2008** in vol.1 no2 omitted our Deputy Chairman **Martin Goosey**

It is the policy of the Journal to correct errors in its next issue.
Please send corrections to :-
bruce.rout@ tiscali.co.uk

Technical News

from **Len Pillinger F.Inst.C.T.**

Legislation & Standards Digest (May 2008)

When I left the employment of BSI Product Services in December, I assumed that my 25 year involvement with Standards development had come to an end. However, I am now attending BSI Technical Committees as a representative of the Institute which means that I can provide members with feedback concerning any relevant legislation or Standards issues through the newsletter in the form of a Legislation & Standards Digest (LSD?!).

The two committees on which ICT is now represented are concerned with PCB and assembly Standards in the case of EPL/501, and environmental issues (RoHS, WEEE, EuP, REACh etc) at GEL/111. To assist in reviewing the documentation I have the welcome support of Dr Martin Goosey (Loughborough University IEMRC) and Mark Drewett (Chemigraphic Limited) who volunteered at the ICT AGM. I also enrolled Peter Starkey in his absence which will give the team a good balance of ICT interest groups. It is no trouble to add more ICT members to the email distribution if you wish to be involved.

Whilst it has been a quiet few months in terms of PCB and assembly standards, RoHS and REACh are causing plenty of controversy.

RoHS Directive – 46 new materials proposed for restriction!

The Öko Institut in Freiburg Germany who describe themselves as "a leading European research and consultancy institution working for a sustainable future" won an eight month contract, which began in October 2007, from the EU Commission to review the RoHS substance restrictions. They have proposed 46 new substances and have been taking comment from industry over recent weeks. It is no surprise to find that industry has commented in a quite robust tone!

You will be equally unsurprised to hear that both TBBA (our workhorse flame retardant for laminates) and Antimony Tribromide (synergist used with flame retardants) are on the Öko hit list. Gallium Arsenide is also targeted which would affect manufacturing of power semiconductors. Beryllium Copper is another candidate which is used extensively for connectors and contact springs. Nickel is a further contender for restriction, and item 46 is Colophony; the naturally occurring resin that is an active constituent in many fluxes.

I have to express considerable admiration for the response sent by the IPC. It is a balanced, intelligent and well argued reaction from Fern Abrams, IPC Government Relations and Environmental Policy Director, which takes environmental and health issues into account whilst recognising materials science, legal and fiscal constraints. ERA Technology has also responded taking each of the 46 substances in turn and offering regulatory and materials science critique. The full story including the complete list and responses can be seen at :-

http://hse-rohs.oeko.info/

but be prepared for information overload.

One concern that has been expressed is that Öko appear to have taken a toxicology-based approach combined with a precautionary principle whilst failing to take proper account of the impacts on industry. Respondents have also questioned the availability of safer alternatives, and whether as much is known about the alternatives as is known about the substances they are replacing. Öko may be suffering from comparison with ERA Technology who conducted earlier reviews and whose approach was seen as being more holistic.

Separately, a collective of NGOs including Greenpeace have submitted a report suggesting a significant reduction in the existing exemptions and exclusions and proposing new substances be restricted.

The only certainty is that this story is going to run and run, with a lot more debate before any changes are made to the legislation.

REACh Regulation

I should begin by noting that the Öko RoHS proposal was couched in terms that are clearly derived from REACh. If the 46 fail to make their way into RoHS, then it is likely that they will be proposed as 'Substances of Very High Concern' (SVHC) under REACh. This is likely to create constraints for their use rather than a ban.

The HSE are running a series of events about REACh, including ones for 'Downstream Users' which includes many organisations in the electronics supply chain. These events are free (including a good buffet lunch!), being organised all around the country and can be seen at www.hse.gov.uk/reach/diary.htm. The events are informative and there is ample opportunity to interact with the experts either from the floor or one-to-one.

If you think that REACh does not affect your organisation, or that 'wait and see' is the best option, I urge you to take a look at www.hse.gov.uk/reach/role.htm.

Artificial Optical Radiation Directive

This is Directive 2006/25/EC and it completely passed me by until a few weeks ago, and I do not suppose that I am alone in this. Although this Directive was approved two years ago, Member States have until the 27th of April 2010 to enact national legislation.

To quote UV Light Technology Limited (and avoid accusations of plagiarism):

"This new EU Directive 2006/25/EC lays down the minimum health and safety requirements for the protection of workers from risks arising from exposure to artificial optical radiation. The term 'optical radiation' defines the region of the electromagnetic spectrum which includes UV, visible and infrared light.

The Directive establishes provisions for the safe use of artificial UV light and is based on the exposure limit values defined by the International Commission on Non-Ionising Radiation Protection (ICNIRP). Currently there are no specific legal provisions covering occupational UV light exposure. Control of exposure is governed by the general provisions of the Health and Safety at Work etc Act 1974 and the Management of Health and Safety at Work Regulations 1999. Inspectors from the Health and Safety Executive refer to the ICNIRP guidelines and the Health Protection Agency (HPA) recommendations when assessing compliance with this legislation.

The Optical Radiation Directive therefore adds little to the existing requirements, however it does define more precisely what is expected. For example, employers must determine personal UV light exposure levels and compare with the exposure limit values as a means of assessing risk and necessary controls. Workers should not be exposed above the exposure limit values and must be provided with specific information and training."

The PCB industry uses processes within the wavelengths described, and so this is another piece of legislation to be taken into account. The exact requirements will become clearer once the UK 'Statutory Instrument' and Official Guidance have been published.

It is not my intention to spread cynicism or depression with this Digest. However, *Regulatory and Compliance Risk* came first in this year's Ernst & Young Strategic Business Risk survey. Information is the first step to limiting business risk.

Len Pillinger F.Inst.C.T

1st May 2008

PCB Design is Easy ?

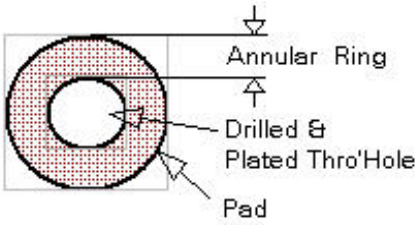
Sue Critcher M.Inst.C.T.
Total Board Solutions Ltd

PCB Design is Easy ? That is the statement that is made to me time and time again, normally followed by the phrase 'you just join the dots!' When I first started in PCB design that probably was true to a point, but in these days with high speed and RF designs the way the 'dots are joined together' can mean the difference between a board working and failing. Gone are the days when a designer could just sit at his/her terminal in a world of their own just happily placing and routing a design without any external information. What do I mean by this? These days a designer has to be aware of more things than just a list of parts and connections. Without this understanding it may not only affect the functionality of the board but also the fabrication, assembly and test. I would love to be able to say that all the designs I have produced have sailed through the fabricator's front end checks and that I have never had a query back, I would unfortunately be lying and I know too many people in the industry to try that one!

So why do we see any issues at all if the latest software systems do all the work for us designers these days? Are we all just bad designers that cannot be bothered to check our work? I do not believe that any designer thinks I will send out a board which I know will fail the front end checks. Why is that? If a board has been sent for fabrication that means the designer is now working on the next design, if he has to stop that to investigate an issue found that means the design at the fabrication house is on hold and so now is the new design which was being worked on. In all the companies I have worked at having a design on hold waiting for your input is a very high profile position to be in, especially as any delay could end up with a slip in the time to market.

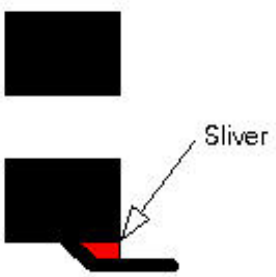
Because of this point alone I believe that every designer thinks the data that they send for fabrication is perfect. So that brings us back to the original question: why do fabrication houses see so many issues? Everyone knows that the software packages these days are so complete that they can check for any errors. Or is that the case? Indeed for most software packages you can buy add on capability that will check your post processed data. For a lot of companies they will not invest in the software. To quote a boss of mine recently 'to do the fabricator's front ending for them!' This extra software can be a cost that is hard to justify especially if you are a small company. So what sort of things regularly go wrong that we can check for without necessarily having to invest in this extra software?

Annular Ring



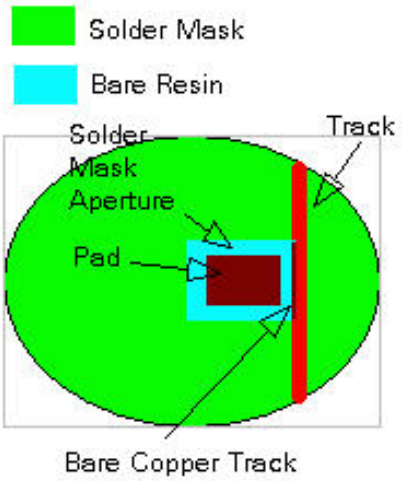
When calculating the size to make a pad for a via or a through hole most designers would check their fabricator's web site or specification for the smallest cost effective annular ring. They would then take the hole size plus twice the annular ring and they have their pad size. THIS IS NOT CORRECT! To get the finished plated hole size the fabricator has to drill the hole larger to plate down to the size we as designers require. Suddenly now your annular ring size is below their recommendations. This misunderstanding comes from the fact that most designers are talking finished hole size where as most fabricators are talking about drilled hole size! Remember to keep this in mind when calculating pad sizes! Fabricators need to inform the designers that they are not calculating their pad sizes using the most cost effective options.

Copper Slivers



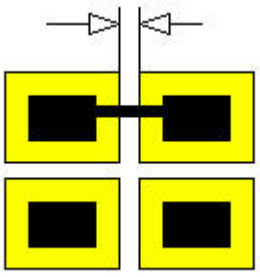
As board density gets greater and-greater the above issues become more and more common. To fit tracking into tight areas designers are sometimes forced to turn from a pad too acutely, and that can leave slivers which come off during board fabrication and in worst case cause an open circuit. Most software systems do allow you to setup a minimum distance a track must be from a pad before it can turn to prevent issues like this occurring. Unfortunately this then stops a design being routed 100%. Again, without the extra software the only check for this is a visual one and designers sometimes miss some or have been forced to design as above.

Solder Mask Exposed Tracks



Suddenly your solder mask apertures are leaving tracks exposed! Why is that? Nothing has changed in your library. That may well be the problem. Most designers are using a library that was created many years ago when the track and gap values were much larger than the ones we are using today. Also, with the shape based routers we have now they place a trace using the pad + clearance dimension, hence you see far more occurrences of the above problem. Designers need to re-visit their libraries on a regular basis especially if their track and gap values are getting smaller. Fabrication houses need to feed back issues like this to the designers or the problem will not go away!

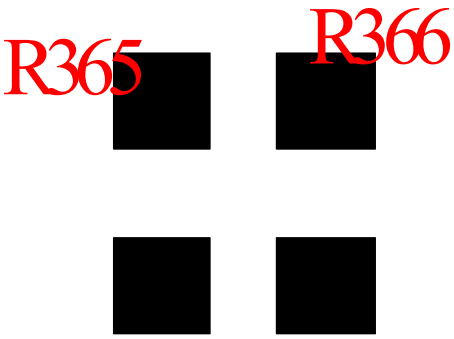
Solder Mask Slivers



placing components closer side by side can cause solder mask slivers. A fabrication house may decide to make this one large solder mask aperture which solves

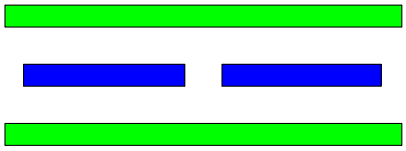
their problems during bare board fabrication. Unfortunately it then causes a problem during assembly as the solder paste can flow from one component pad to another! If a fabrication house sees this issue they must speak to the designer before going ahead. The problem again will be caused by an out of date library, or maybe an incorrect library with for example a set of pads that are so close together individual solder mask clearances are not possible and you need to block out a complete set of pads.

Silkscreen Issues



On many boards these days there is no room for silkscreen or only the active components have silkscreen identifiers not the passive ones. In any case, the problem you see above is far too common. Again why does this occur? Well, the silkscreen text within most software products is attached to the geometry. This means that all pieces of silkscreen text come in at the same position relative to the geometry. Once within the design it is up to the designer to manually move all pieces of text so that they do not overlap any pads. We are only human!! This is probably one of the last things we do before post processing the job which means we have a project engineer shouting at us to get the data to the fabrication house as soon as possible! This is no excuse; most software packages have a silkscreen clipping option which a lot of designers do not use, as some software packages do not allow you to say what to clip and what to ignore. This could mean that the silkscreen ends up illegible. If fabricators find issues with silkscreen they need to feed it back to the designer. If not when you get a new revision of this design the errors will still be there.

Impedance Matched Traces



There are many tools out there for calculating the impedance of a copper track. What all these tools have in common is that they ask for the dielectric constant value of the material that you will be using. This value can be different between one fabrication house and another and needs to be confirmed with the fabrication house making your board. Next you need to specify the board stackup that you will be using including the distance between relevant layers. You can add any values you like for these and the tools will calculate the trace widths and gaps required, but to achieve the stackup you specify may not be the most cost effective build for your board or even in the worst case may be unmanufacturable ! So again before using these tools please confirm all the values you are going to enter to make sure they are cost effective to produce.

In conclusion what I am trying to say is that talking really works! If you are a designer reading this then please try and get a good relationship going with your fabrication house. In this way you will get to know any issues he has with your designs and you will learn from this experience even if in the beginning you feel that nothing you produce is right!

If you are a fabricator do not cover up issues you find with designs, if designers are not told of any issues with their designs you will see the same problems on any future issues of the design or in worst case if that design becomes a board that is copied for future designs you could see the issues every time you receive anything from this company. I know it is easier to put these things right than getting the reputation of being an awkward fabricator but that would be overcome by building a good relationship with the designer so they know that all your suggestions are worthwhile.

In both cases if you are either a fabricator or a designer try to put yourself in each other's shoes for a while before you assume that the other person is just stupid or awkward ! I cannot say how much difference it makes to cost effective design if you have a good working relationship with your fabricator. To involve them early in a design process gives them a good heads up of the type of designs you are producing and they have a wealth of knowledge that you can call upon. For fabricators, instead of the first time you see a board being when you receive the Gerbers, you can assist the designers to produce something that would be easier to fabricate.

So please learn from my experience: a good working relationship can make or break a board design.

Sue Critcher
Total Board Solutions Ltd

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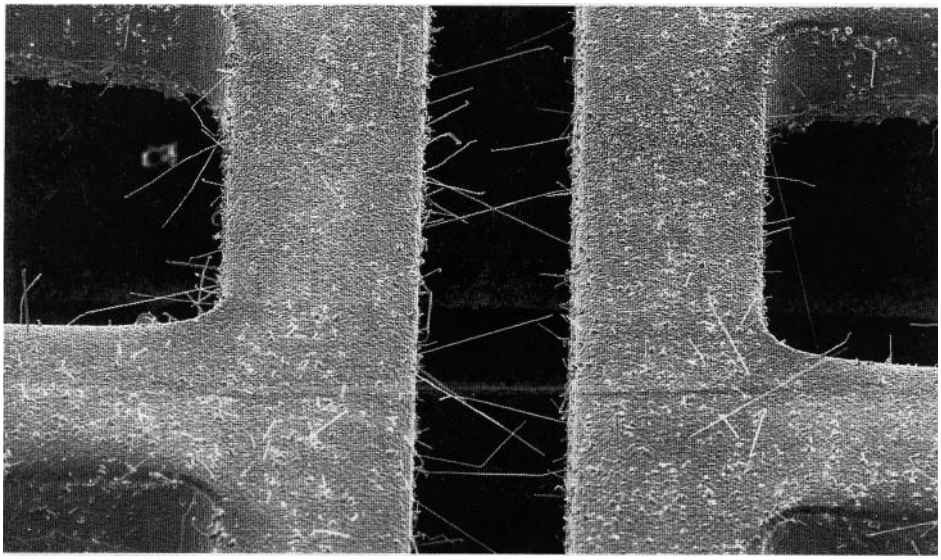
Within a whisker of failure

Removing lead from solder may have seemed a smart idea environmentally, but the resulting microscopic growths called tin whiskers could be just as problematic, says **Kurt Jacobsen**



On April 17 2005, the Millstone nuclear generating plant in Connecticut shut down when a circuit board monitoring a steam pressure line short - circuited. In 2006, a huge batch of Swatch watches, made by the eponymous Swiss company, was recalled at an estimated cost of $1bn (£500m). In both cases, "tin whiskers" - microscopic growths of the metal from the soldering points on a circuit board - were blamed for causing the problem.

It's not the first time these mysterious growths have been blamed for electronics failures. In 1998 the Galaxy IV Communications satellite sputtered out after just five years; engineers diagnosed its failure as due to "whiskers".

The US military blamed them for malfunctioning F-15 radar systems and misguided Phoenix and Patriot missiles. In 1985, the US Food and Drug Administration recalled a number of pacemakers because of these same whiskers (tinyurl. Com/28dxx8). In fact, they've been known about since the 1940s, and happen with cadmium and zinc, too: during the second world war, similar whiskers would short the cadmium tuning capacitors in aircraft radios. A decade later, tin-based relays in AT&T telephone switching centres were found to cause shorts.

Pushing tin

The solution to "whiskering"? Mix lead into the solder, as was done from the 1950s. Colin Hughes, a physicist who worked on the first British nuclear bomb, told me that the whiskering problem never came up during his career.

But now the lead is gone, by legal mandate, and whiskers are back – causing potential problems for us all.

Since 2006, lead has been banned from solder in the European Union under the 2003 Restriction of Hazardous Substance (RoHS) directive, which gave manufacturers three years to phase out lead.

The logic seemed reasonable. Removing lead from petrol (where it was used to prevent engine mistiming) brought clear environmental and health benifits, taking a harmful chemical that can affect intelligence out of our atmosphere. Removing lead from solder, the 37% lead,63% tin alloy used to join metal objects in everything from plumbing to circuit boards, was an obvious next step to prevent it leaching into ground water from dumped items in landfills.

Meanwhile, the US and Japan have also been moving to lead-free solders. It's a huge shift; the US Environmental Protection Agency (EPA) estimates that 80m kilograms of lead solder was used worldwide in 2002. Environmental groups have applauded the move. "In the US we've been survivng without lead solder for many years," says Rick Hind, legislative director of Greenpeace's toxics campaign. "With less exposure to lead we will all benefit by being smarter and making safer and more durable products." (The US has not made lead-free solder obligatory, but does offer tax benefits for doing so.)

But without lead to tame it, tin behaves oddly on circuit boards. Left alone, tin plating, like cadmium and zinc, spontaneously generates microscopic shreds of metal - about one to five microns in diameter, or less than one-tenth as wide as a human hair - which push up from the base. If they grow far enough to touch another current carrying location, they'll cause a short that can wreck the equipment while leaving barely any trace.

The cause is becoming clearer. " I believe the mechanism of whisker formation is now understood: it is due to compressive stress - caused by, say, diffusion of copper into the tin - being built up in the tin layer which breaks through the tin oxide barrier layer [to the air], " says Steve Jones of Circatex, in South Shields. Critics cite reports that solder substitutes – pure tin, tin-zinc, tin-silver-copper – simply cannot match the lead mixture for realiability, coverage ("wetting" terminals), and cost (silver is especially pricey). Therefore, the US Military, Nasa and medical and highlevel research equipment are exempt from what authorities view as untrustworthy commercial components.

"I still use tin-lead solder – it works better," says John Ketterson, a solid state physicist at Northwestern University in Illinois. He notes the tradeoffs of "cost, materials, strength of the solder, and all that" during this mandated changeover, and that manufacturers "have to get an experience base" with new processes.

Double standards

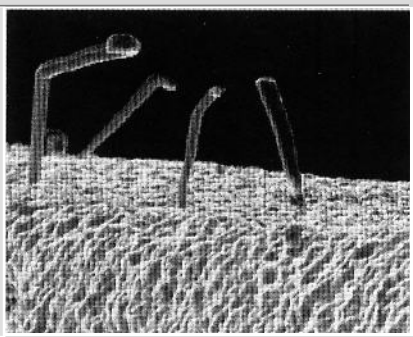
This means the unwitting consumer bears the cost of the experimental burden. " So Nasa does not want the economic risk of having the Hubble [Space Telescope] go down. But if one personal computer in a thousand goes down because of whiskers, no one is going to do much about it," says Ketterson.

One in a thousand may be a generously low estimate. Besides whiskering, lead-free solder is more brittle. Substitute solders also may be applied too thinly or with too little heat - or, for that matter, with too much heat (lead substitutes have higher melting points), stressing the circuit board laminate.

The question is, are the products we are using now being affected by tin whiskers? When your computer >>8

Tin whiskers: coming to a PC near you?

They can grow at ambient temperature and humidity, or in vacuum
They can grow in steady or varying temperatures (though the latter may encourage growth)
Whiskers' tips are atom-sharp. They will push through any coating, given time
They are a prevalent cause, only now being identified, of many past equipment failures
One whisker can carry about 30mA - more than enough to cause havoc in digital circuits
Silver-tin-copper ("SAC") solder slows but doesn't stop whisker growth
SAC solder has more environmental impact than the lead-tin version



Older 37%-63% lead-tin solder mix merely deforms, reducing stress and hence minimising whiskering
Whiskers can grow indefinitely

Source: Howard Johnson, Signal Consulting

stops working, could that be the cause? Certainly, some in the computer industry know about it: representatives from Sun Microsystems and IBM were among those presenting at a tin whisker workshop in 2006 ; a second is due later this month.

Using a matt finish, removing contaminants from the solder and surfaces, and reducing mechanical stress on the components being soldered all mitigate the growth of whiskers. But Bob Willis, an opponent of the EU directive and technical director for the SMART (Surface Mount and Related Technology) Group in the UK, says that so far there is "no definite solution to the problem".

More than 80% of all electronic components are made in Asia but specifications are imposed by the brand-name company. I rang eight manufacturers to enquire about encounters with whiskers and related problems. Only one tech support person - and no spokesperson - knew anything about it. Yet Google "tin whiskers" and you get 40,000 hits.

Apple was the only manufacturer to respond, stating that the company "has been using lead-free solders since 2004 without issue". Perhaps manufacturers haven't developed an "experience base", or perhaps it isn't registering as a problem. Many customers will probably chalk failed devices off to their own isolated tough luck, when the cause might really have been microscopic whiskers inside their machines.

Lessons learned

Overall, was it sensible to go lead-free? "I would say no," says Willis. Earlier obsolescence means more discarded devices. Critics argue that substitutes are more toxic and energy-wasteful than the lead they replace - and that lead doesn't leach from circuit boards, because it doesn't migrate as lead in paint or petrol does.

The National Electronics Manufacturing Centre for Excellence, sponsored by the US Navy, did find that modifying the temperatures at which soldered items are bathed and stored diminished whiskering, but nevertheless recommends the "use of lead in conflict with future industrial practice." And Swatch, after its expensive recall, won a permanent exemption from the RoHS directive for its exports to the European Union.

Perhaps a reliable lead-free process will be conjured up soon - though experts doubt it. Companies such as IBM and National Instruments say they are now achieving RoHS compliant techniques even for exempt products. But this debate among professionals looks like it needs to come out in the open. So far, the last source to count on for information about this looming problem is the manufacturers.

This article appeared in
the**guardian**Thursday 03.04.08
and is reproduced with their permission

Letters and e-mails

The following letter appeared in the Guardian April 17 2008

Tin woes solder on

Congratulations on the very interesting Article on tin whiskers. You may be interested to hear of another phenomenon associated with lead-free solders in electronics, known as tin pest. Research was carried out into the allotropy of tin 80 yeas ago. Tin pest was found to occur by a process of nucleation and growth of "grey" tin (a form found below 13C), and was very slow – often requiring years to complete. Since the transition from "white" to "grey" tin involved a 27% increase in volume, its function was restricted to the surface. Recently, tin pest has been reported in bulk samples of lead-free solder alloys following a few years' exposure at -18C, the usual freezer temperature.

To date it has not been observed on actual joints. But lead-free interconnections have been in service for a relatively short time. Although we do not know whether it is necessary to shut the stable door, we should make effort to understand and control tin pest formation. Only time will tell whether it represents a real problem in electronics.

Professor Bill Plumridge, *Faculty of Technology, The Open University*

Foundation course in PCB Design and Manufacturing

Report from Delegate to Sponsoring Company

First of all I would like to thank you for sending me on the course, it was very interesting and I really enjoyed it. Foundation Course in PCB Design and Manufacturing took place mainly at Loughborough University in Leicestershire from Monday 31st of March 2008 to Thursday 3rd April 2008.

The whole course was well organized and every thing was in the right place. First day we were in Tamworth where we could also visit the Invotec factory which I think was very good idea to see how it looks in practice. After that we went to Loughborough University in Leicestershire where we based for the rest of the course.

This course gave me a chance learn and also see how to manufacture PCB from the beginning to the end and how they are designed.I learnt lots of useful things like what types of laminates can be used, how to programme, drill and route, plate through holes, how to prepare surfaces and what is the most important step on that process.

The course gave me improved understanding about the soldermask technologies, why we use them, the application techniques and surface finish. Most of the lectures were well prepared.

The course gave me a deeper understanding of how Electra's products are used by their customers.

Foundation Course in PCB Design and Manufacturing gave me a chance to met lots of nice people and learn lots of useful things, which will help me to improve where possible.

Agnieszka Wozna *May 6 2008*
Electra Chemicals & Polymers Ltd. - Delegate at Foundation Course 31st March - 3rd April

Integrated Optical and Electronic Interconnect Printed Circuit Board Manufacturing

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1. Introduction

At high bit rates copper tracks in printed circuit boards (PCBs) suffer severe loss and pulse distortion due to radiation of electromagnetic waves, dispersion and bandwidth limitations. The loss can be overcome to some extent by transmitting higher power pulses and by changing the dielectric constant and loss tangent of the PCB substrate material. However, high power pulses consume power and can cause electro-migration which reduces the board lifetime, although the copper tracks can be surrounded by another metal to prevent this at the expense of further processing steps. The use of special board materials can be costly and some materials containing high dielectric constant crystallites can cause poor adhesion. The pulse distortion, dispersion and bandwidth limitations can be overcome to some extent by the use of pulse pre-emphasis and adaptive equalisation at further cost. Electromagnetic waves are radiated efficiently at high bit rates removing power from the track so causing loss, but more importantly they are also received efficiently by other nearby and distant copper tracks on the same PCB, or on adjacent PCBs, or PCBs and other electrical conductors outside of the system enclosure. This EMI crosstalk causes increased noise and so degrades the signal to noise ratio and the bit error rate of the copper track interconnections. Therefore, the main forces driving the development of alternative interconnect technologies are the EMI crosstalk, which becomes increasingly more serious as bit rates increase for longer and denser interconnects, and secondly the cost of overcoming the other problems that occur in copper interconnects at high bit rates.

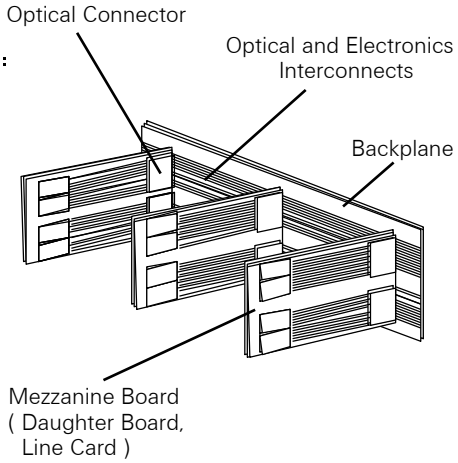


Fig.1: Schematic view of backplane Architecture.

Optical fibres have replaced copper cables for long distance, backbone and submarine applications where they offer wide bandwidths for low loss, produce and receive no electromagnetic interference, and are relatively low cost. Optical interconnects are beginning to penetrate the markets at shorter distances, such as in local area networks, and as their cost is reduced, will be used within the system enclosure.

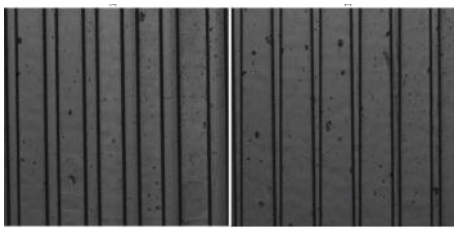


Fig.2: Photolithographically fabricated straight and tapered waveguides of a range of widths and taper ratios

The use of optics is expected to occur first where the problems for copper are most significant which is for high bit rate, dense interconnections in large area backplanes within non-conducting enclosures. Optical fibres are not the most convenient for interconnections within a system as they can only bend through a large radius of about 10 cm, otherwise light escapes from the fibre core into the cladding resulting in loss and signal corruption. Fibre connectors form a major part of the cost of the optical interconnect and a system with many fibres has many costly connectors. The fibres must be individually routed and errors in routing are time consuming to debug and correct. The fibres can be laid flat on the PCB plane and even bonded together within an epoxy layer, but this is not suited to low cost mass production. An alternative technology suitable for low cost mass production is that of multimode polymer buried channel optical waveguide interconnections within layers in the multilayer PCB formed by the same, or slightly modified, processes already available within PCB manufacturing facilities. Copper tracks are still required in such substrates to transmit power through the backplane (or motherboard), Figure 1, in order to power mezzanine (or line, or drive, or daughter) boards and copper is still a practical and low cost option at low data rates.

Hence, there is a need to develop a new type of multilayer hybrid PCB in which optical waveguide interconnects are used for the highest data rates, with copper tracks for lower data rates and for power lines and earth planes. These issues have been anticipated by system design companies such as Xyratex Technology, IBM Zurich and Siemens C-Labs, microprocessor designers such as Intel and materials development companies such as Dow Corning, NTT, Rohm and Haas and Exxelis, who have instituted research in their own laboratories and in associated universities into optical waveguide interconnect technology.

Leading Universities and Research Institutions such as Cambridge (CAPE), University College London (UCL), Heriot Watt University, Loughborough University, National Physical Laboratory (NPL), IMEC - Ghent University, TFCG Microsystems, Belgium, Paderborn University, Germany, Helsinki University of Technology, Espoo, Finland and ETRI, South Korea are developing novel polymer materials, developing fabrication techniques, discovering design rules for waveguide layout and carrying out precision characterisation.

Optical buried channel waveguides usually have a core with an approximately square or rectangular cross section made from a high refractive index (slow speed of light) material and a cladding surrounding the core of a lower refractive index (higher speed of light). They operate by total internal reflection (TIR) in a similar way to optical fibres. The cost of waveguide connectors is minimised by choosing to use multimode waveguides which typically have cores of 40 - 70micron width which can tolerate more misalignment than single mode waveguides. The optical buried channel waveguides are formed

on a plane by a variety of fabrication techniques which can be implemented, after slight adaptation, in PCB manufacturers. Arrays of low-cost vertical cavity surface emitting lasers (VCSELs) emitting 850 nm wavelength and arrays of photodiodes operating at 10 Gb/s are readily available at low-cost for use in optical transmitters and receivers. At this wavelength, polymer is a convenient low-loss material for use as the core and cladding. Polymers can be chosen or designed which can be easily processed to form waveguides at low temperatures, have low cost, and can withstand subsequent high temperature reflow soldering processes.

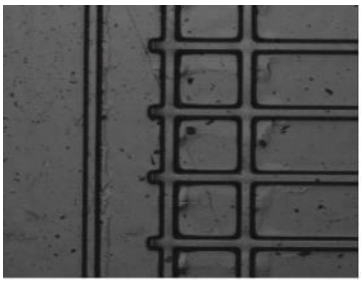


Fig 3: Photolithographically fabricated 90º waveguide crossings

For optical printed circuit boards to be brought into widespread use, layout tools must be made readily available which design both the copper tracks and the optical waveguides [1]. In 2006 David R. Selviah of UCL, formed a large consortium of complementary universities and companies and led a successful bid to carry out a Flagship project entitled "Integrated Optical and Electronic Interconnect PCB Manufacturing (OPCB)" in the Innovative Electronics Manufacturing Research Centre (IeMRC). The consortium companies represented a complete supply and manufacturing chain and route to market for the polymer waveguide technology including companies manufacturing PCB layout tools, computer programs for modelling the behaviour of multimode waveguides, developing and supplying low loss polymer formulations, manufacturing multilayer PCBs, supplying printer fabrication equipment together with end user system companies who require optical printed circuit boards. The following sections describe the project's objectives, the approaches being taken and some examples of what has been achieved so far in the project with an indication of future directions.

2. The OPCB Project's Objectives

This three-year research project is exploring novel methods, compatible with traditional multilayer PCB manufacturing processes, for the manufacture of optical waveguides capable of operating at very high data rates within an optical layer in the PCB. Several process routes are under investigation, each with different levels of risk and cost. In addition, modifications are being researched for commercial computer aided design software for PCBs to allow them to also layout optical waveguide patterns. The detailed objectives are:

(a To establish waveguide design rules for several different manufacturing techniques and to incorporate them into commercial design rule checker and constraint manager layout software for printed circuit boards so that PCB designers can easily incorporate optical connection layers without detailed knowledge of the optics involved. To investigate and understand the effect of waveguide wall roughness and cross sectional shape on the behaviour of light and the effect on waveguide loss.

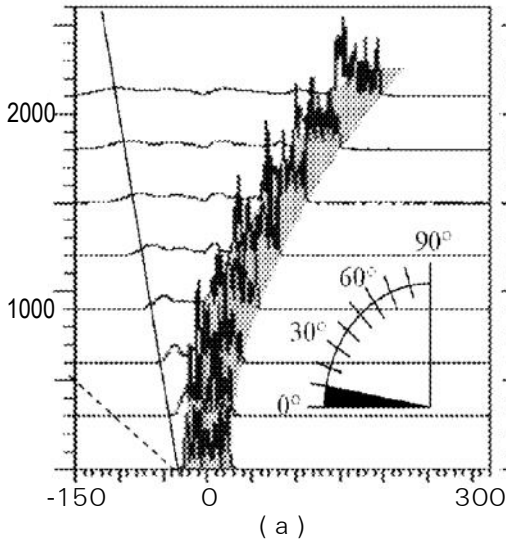
(b) To develop low cost manufacturing techniques for integrated Optical and Electronic interconnected Printed Circuit Boards, OPCBs. To develop and to compare the commercial and technological benefits of several optical printed circuit board manufacturing technologies – photolithography, direct laser-writing, laser ablation, embossing, extrusion and ink-jet printing – for high data rate, small and large (19"), rigid and flexible, printed circuit boards so that it will be clear which technology is best for each type of PCB. To characterise the behaviour of optical waveguide backplane systems in real world conditions, including temperature cycling, high humidity and vibration.

(c) To design a commercial, low cost, optical connector (dismountable, passive, self-aligning, mid-board) as the next stage from the prototype demonstrated in an earlier project (Storlite Project). To develop novel connector designs suited for interfacing flip chip lasers and photodiodes to OPCBs, and OPCBs to OPCBs through a right angle connector.

3. The Consortium

The consortium consists of 3 universities and 10 companies. Dave Milward of Xyratex Technology acts as Industrial Project Manager, while David R. Selviah of UCL is the project Technical Leader.

The funding for the project is provided by EPSRC through the IeMRC and by the consortium industrial partners amounting to a total of £1.3 million over 3 years. The EPSRC funding is divided between the 3 universities who carry out the bulk of the research described in subsequent sections.



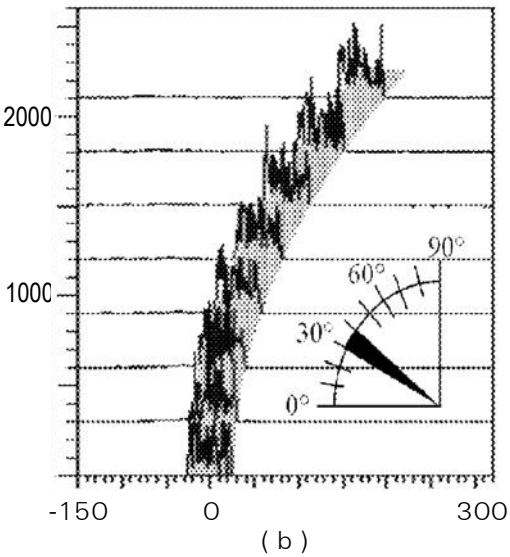


Fig 4: Computer simulations of the optical field in a 90º waveguide bend
(a) at the start of the bend after a straight input waveguide showing radiated light beyond the outside of the bend,
(b) a third of the distance along the bend

4. Waveguide Layout, Modelling and Characterisation

University College London (UCL) lay out waveguide test patterns and system demonstrator waveguide interconnection patterns using modifications they have made to Cadence software layout tools. Their experimental measurements of these waveguide components after fabrication, Figures 2 and 3, in various polymers using a range of fabrication techniques are compared to their computer modelled results in order to gain a detailed understanding of the physical

behaviour of coherent light in multimode waveguides and so to establish design rules [2-10]. Figure 4 shows an example of the modelled field in a multimode waveguide bend. A novel theory is being developed for analysing the effects of waveguide side-wall roughness. Low-cost, self-alignment techniques are being developed for use in optical connectors for aligning lasers and photodiodes to waveguide end facets and the misalignment tolerances are being assessed. UCL, as lead university, forges international links with other waveguide researchers such as in their recent mutually beneficial visit to IMEC - Ghent University, TFCG Microsystems, Belgium and promotes and disseminates their own [2-10] and the consortium's results [13-14] via a range of international conferences and journal articles.

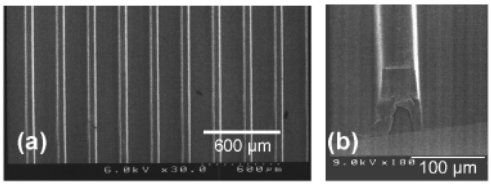
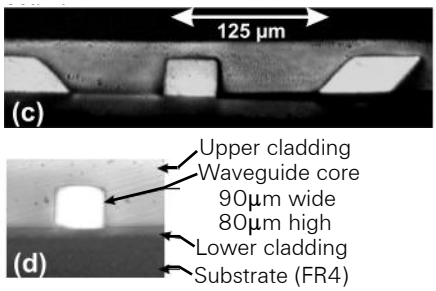


Fig 5: The SEM images in (a) show Directly written, unclad polymer waveguides (~50 x 50µm) on a glass substrate. The guides are on a 250µm pitch and the cross-section of one of the guides is shown in (b) - It was cut using a scalpel blade. The optical microscope images in (c) & (d) show end-on views of back-illuminated cladded structures fabricated on FR4 substrates - those in (c) were fabricated using a normal and ±45 angled beams having a flat-top intensity profile. The core shown in (d) was written at 30 mm/s using a focussed Gaussian beam.



5. Laser Direct Writing of Waveguides

Heriot-Watt University [11,12] has previously developed a direct UV-laser-writing technique so as to form multimode polymer waveguides. In the OPCB project, the key aim is to explore how these techniques can be extended to suit optical backplane applications – both in the context of scale and manufacturability. Fabricating waveguides over metre-scale boards requires not just the ability to write over large areas but also, if production time is to be minimised, faster writing speeds e.g. >50 mm/s. The HWU group has set up a laser-writing facility capable, in principle, of operating over an area 300 mm x 600 mm at up to 1 m/s. Using this system, they have been working on the challenge of writing well-defined, low-loss waveguides very much faster than the 100 ìm/s write speeds typically used in previous work, Figure 5. Using laser spots with tailored intensity profiles and an optimised photopolymer formulation, recent results have demonstrated speeds of around 50 mm/s, for writing 50ì m multimode acrylate waveguides. Both straight and curved guides can be fabricated. The HWU group is also exploring fabrication techniques by which their proven techniques for creating embedded 45º out-of-plane mirrors, Figure 5, can be made compatible with large board processing.

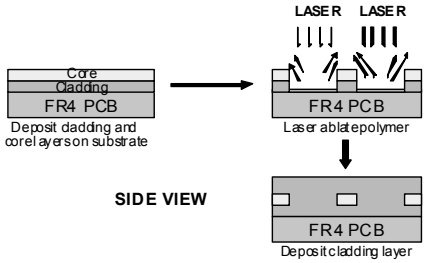


Fig 6: Schematic diagram of laser ablation for the formation of waveguide structures.

Fig 7: Plan view of ink jet deposited optical waveguide material on a modified glass surface (track is approximately 75micron wide).

6. Laser Ablation and Inkjet Printing of Waveguides

Loughborough University is investigating the laser ablation of polymer materials to form waveguides (fig. 6). Two routes are being investigated: the first involves the use of a commercial Nd:YAG system, based at an industrial partner, to machine waveguide structures. This method is attractive as it is utilising equipment already established in PCB manufacturing facilities for the drilling of microvias and therefore would not require additional capital investment. The effect of machining parameters on the depth and speed of ablation is being investigated, together with wall roughness. The second approach considers the use of an excimer laser to form waveguides. However, as this type of laser can use a mask projection technique to shape the beam spot, the fabrication of more complex 3D terminations, such as curved mirrors at the end of the waveguides, is also being investigated.

A significant aspect of the research at Loughborough covers the use of ink-jet printing to deposit polymer waveguide materials. This has the potential to enable fast printing over large areas. For ink-jet fabrication, a potential process route is expected to consist of the initial deposition of a cladding material layer, onto which the core material is jetted to create the appropriate waveguide structure. This will then be enclosed in a further layer of cladding. In order to create core structures with appropriate dimensions and cross-section, the viscosity and surface tension of the jettable core material is crucial in achieving optimum results. Furthermore, the interaction of the ink-jetted material with the substrate is key in determining the wetting behaviour and the stability of the liquid as-deposited structure.Fig 7 shows a line of UV curing optical waveguide material ink-jet deposited onto a glass substrate for which surface modification was carried out to control the wetting, enabling a feature approximately 75microns wide and15 microns high to be formed.

7. Conclusions

The research being carried out within the IeMRC OPCB project by the 13 member consortium addresses a wide range of problems that need to be solved before multimode polymer waveguide technology becomes widely available. The research ranges from formulation of novel polymers to development of new processes and methods for deposition and patterning of the materials suitable for large area substrates and applicable to PCB manufacturing environments. The characterisation and modelling of these structures will lead to the establishment of design rules for optical waveguide components such as bends and tapers which can be implemented within design and layout software tools, further aiding the uptake of this technology. Further details of the research can be found in [13-16].

8. Acknowledgments

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The Membership Secretary's notes May 2008

The Institute now has in excess of 225 Members, drawn from all parts of our Industry; an Industry which is stabilizing across Europe, and increasingly seeing the benefits of belonging to an organization which exists solely for its members.

We are providing six evening Seminars, two Symposia and a one-week foundation course as well as our quarterly journal this year and I would like to thank everyone who is supporting us at these events.

We would like to send our congratulations to **Rex Rosario**, who has been elected to the board of the **IPC.** Rex is one of our longest serving members and is also the Chairman of the EIPC, a platform which will enable him to champion the cause of the European PCB Industry.

Soldertec Global/Tin Technology has announced their Annual Lead-Free Solder Awards and **Bob Willis** proudly receives the 'Process Development Award', in recognition of his many achievements and enthusiasm in assisting industry in the preparation for the implementation of lead-free legislation. Bob coordinates the SMART Group activity for the EU project LEADOUT, currently Europe's largest funded research project. Bob has been a Council Member of the ICT for many years.

Walt Custer is also in the news again. Prior to his Keynote speech to the Wallstreet Journal, Walt was introduced, not as plain old Walt Custer, or even the famous Walt Custer. Apparently, he is now the **very** famous Walt Custer!

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