Journal of the

Institute of Circuit Technology

Contents

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2008 Events

24/25th January	*EIPC Winter Conference,Rome*
6/7th February	*Southern Manufacturing & Electronics FIVE, Farnborough, Hants*
12th February	14.00 Council Meeting 17.00 AGM 17.30 Evening Seminar, all at White Swan Hotel, Arundel. Supported by Eurotech Group plc
4th March	17.00 Evening Seminar, Davenport Hotel, Darlington.
16/22nd March	*6th EIPC Technology Trip, Shanghai, China.*
18/19th March	*Midlands Manufacturing Technology 08 Exhibition, Ricoh Arena, Coventry*
31st March / 3rd April	Annual Foundation Course, Loughborough University.
22nd May	12.30 Council Meeting - London Canal Museum
29/30 May	*EIPC Summer Conference Dresden*
3rd June	34th Annual Symposium, Tweed Horizon Centre, Newtown, St.Boswells.
3rd July	*PCB Inspection & Quality Assessment – Practical Solutions - St Albans askbobwillis.com*
4th July	*IeMRC Annual Conference - Loughborough*
10th July	11.30 One Day Symposium, The Mead Inn, Denmead, nr Waterlooville, Hampshire. Supported by Cookson Group.
5th August	15.00 Afternoon Seminar, Design Suite, Loughborough University
3rd September	17.00 Evening Seminar, Davenport Hotel, Darlington
14th October	*IMF,Surface Preparation & Pre-treatment, Prior to Surface Finishing, Birmingham Medical Institute*
18th November	14.00 Council Meeting 17.00 Evening Seminar, - Norfolk Hotel, Arundel

Editorial

The Team

As a keen football fan, I was most intrigued by the recent disclosure to the press of a confidential paper written by Arsene Wenger, Manger of Arsenal Football Club as a prompt to a team meeting. It struck me as it did to many that the message can of course apply to business and none more so than our own industry. The people that work in our industry, the team players, are our company's strength, our industry's strength and those that belong to the ICT are all part of the strength of our Institute. The following words can apply within our own professional sphere not just to a premiership football club.

a) A team is as strong as the relationships within it.
b) The driving force of a team is its member's ability to create and maintain excellent relationships within the team that can add an extra dimension and robustness to the team dynamic.
c) This attitude can be used by our team to focus on the gratitude and the vitally important benefits that the team brings to our own lives. It can be used to strengthen and deepen the relationships within it and maximise the oportunities that await a strong and united team.
*d) **Our team becomes stronger by:***

Displaying a positive attitude on and off the pitch
Everyone making the right decisions for the team
Have an unshakeable belief that we can achieve our target
Believe in the strength of the team
Always want more - always give more
Focus on our communication
Be demanding with yourself
Be fresh and well prepared to win
Focus on being mentally stronger and always keep going to the end
When we play away from home, believe in our identity and play the football we love to play at home
Stick together
Stay grounded and humble as a player and as a person
Show the desire to win in all that you do
Enjoy and contribute to all that is special about being in a team - don't take it for granted

Of course, individual results may vary, but the objective is to be top of the league or close to, which requires a consistency of performance and a culture of continuing improvement as the competition is tough and highly competitive.

Steve Payne Cirflex Technology Ltd.

Membership

New members voted into membership by the Council

17 th September 2008

Members (M.Inst.C.T.)

Duane Mackenzie	10116
Alan Rogers	10118
Eric Hinsley	10121

Fellows (F.Inst. C.T.)

Paul Comer	10115
Tom Brown	10117
Les Round	10119
Richard Houghton	10120

Member regraded

Les Blakeman **M.Inst.C.T.** 10049

Corrections and Clarifications

No items have been submitted for correction.

It is the policy of the Journal to correct errors in its next issue.
Please send corrections to :-
bruce.rout@ tiscali.co.uk

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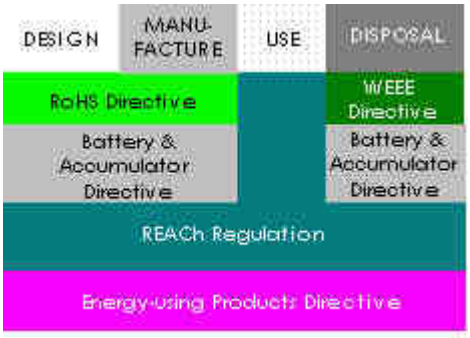
Technical News

Len Pillinger
(The Institute of Circuit Technology representative at REACh)

Legislation & Standards Digest (August 2008)

The European Commission's appetite for environmental regulation continues unabated. I previously reported on the significant controversy over the proposal to add 46 new substance restrictions to the RoHS Directive. The REACh Regulation is now with us, and for ICT members who are part of the electronics design community, there is the Energy-using Products Directive (often amusingly referred to as EuP!) to consider. It is a struggle to visualise how all this legislation fits together, but I believe that this diagram is a reasonable representation of how it fits into the electronics product lifecycle.



Standby Power – is it all Greek to you?

Electronics designers need to take a look at the proposed "Standby and off-mode power consumption Regulation" recently circulated by BERR (former DTI). Why is the EU bothered by such trivia? The official EU figures for 2005 demonstrate that this is anything but a trivial issue:

No. of appliances in Europe having a standby mode	3.7 x 10^9
Watt-hours pa consummed by 'standby' in Europe	4.7 x 10^{12}
Cost of Energy consumption used by standby	€ 6.4 x 10
Resultant CO_2 emissions	19 x 10^6 tonnes

These are big numbers with too many noughts to sensibly visualise. To put the second statistic into context, the total Greek national power consumption in 2005 was a comparable 49 x 10^{12} Watt-hours! (Hence my somewhat facetious heading.)

The EU is therefore proposing this Regulation to address the issue with the aim of reducing standby power consumption by about 35 x 10^{12} Watt-hours by the year 2020 when the number of appliances with a standby mode is expected to have risen to 4.6 x 10^9 appliances.

Presumably this will require some redesign of standby circuits and the associated displays. An unlikely alternative is that mankind gives up its addiction to the ubiquitous remote control and we all get up from the couch to change channel, adjust the volume etc. The range of equipment mandated is limited to the domestic environment:

1. Household appliances:

   Washing machines,
   Clothes dryers,
   Dish washing machines,
   Cooking:
   Electric ovens,
   Electric hot plates,
   Microwave ovens,
   Toasters,
   Fryers,
   Grinders, coffee machines and equipment for opening or sealing containers or packages,
   Electric knives,
   Other appliances for cooking and other processing of food, cleaning, and maintenance of clothes,
   Appliances for hair cutting, hair drying, tooth brushing, shaving, massage and other body care appliances,
   Scales

2. Information technology equipment intended primarily for use in the domestic environment.

3. Consumer equipment
   Radio sets,
   Television sets,
   Video cameras,
   Video recorders,
   Hi-fi recorders,
   Audio amplifiers,
   Home theatre systems,
   Musical instruments,
   And other equipment for the purpose of recording or reproducing sound or images, including signals or other technologies for the distribution of sound and image other than by telecommunications.

4. Toys,leisure and sports equipment:
   Electrictrains or car racing sets
   Hand-held video game consoles,
   Sports equipment with electric or electronic components,
   Other toys, leisure and sport equipment.

Clearly, this can not happen overnight and so a phase-in has been proposed:

	Maximum Power Consumption	
	2010	**2013**
Off - mode power	1.0 W	0.5 W
Standby power without display function	1.0 W	0.5 W
Standby mode with display function (eg: clock)	2.0 W	1.0 W

Manufacturers will be legally required to undertake conformity assessment of new designs including providing documentation detailing for each standby and/or off mode:

- ✓ The power consumption data in Watts rounded to the second decimal place
- ✓ The measurement method used
- ✓ Description of how the appliance mode was selected or programmed
- ✓ Sequence of events to reach the mode where the equipment automatically changes modes
- ✓ Any notes regarding the operation of the equipment

Design for the Environment just got tougher and now has teeth. If you are affected by EuP, then keep a close eye on www.berr.gov.uk/sectors/sustainability/eup/page38894.html

To support this increasingly complex area of legislation; Standards for ecodesign are now appearing. I note the recent publication of BS EN 62078 *Audio / video, information and communication technology equipment. Environmentally conscious design.*

Latest Information on REACh

There have been a couple of significant recent developments. The European Chemicals Agency (ECHA) in Finland has published a guide on REACH for "producers and importers of articles". Remember; a PCB can be defined as an article, as can a PCB assembly. All the official guides can be downloaded from http://echa.europa.eu/reach/fact_sheet_en.asp. The guidance runs to 118 pages which is a model of brevity compared to the REACh Regulation itself!

ECHA have also published the first list of candidate SVHCs; these 'Substances of Very High Concern' will be subjected to the strictest level of regulation. The list can be seen at http://echa.europa.eu/consultations/authorisation/svhc/svhc_cons_en.asp with electronics appearing to get off lightly. The substances nominated to date are:

Substance	Typical use
Anthracene	Semiconductors
4.4 Diaminodiphenylmethane	Polyeurethane production
Dibutyl phtalate	softener / plasticiser for PVC & other plastics, printing inks, film coatings
Cyclododecane	Production of HBCDD Flame Retardant, polyamides, polyesters, oils and solvents
Cobalt dichloride	Drying agent in coatings and inks, used in galvanoplasty
Diarsenic pentaoxide	Hardening copper
Diarsenic trioxide	Starting point for the preparation of arsenide semiconductors
Sodium dichromate, dihydrate	Used by 43% of companies with metal finishing activities
5-tert-butyl-2,4,6-trinitro-m-xylene (musk xylene)	Perfumes / cosmetics. No electronics usage identified
Bis (2-ethyl(hexyl)phthalate) (DEHP	PVC plasticizer
Hexabromocyclodecane (HBCDD)	Flame Retardant, particularly various forms of polystyrene (eg: HIPS)
Alkanes, C10-13, chloro (Short Chain Chlorinated Paraffins)	Metal working lubricant
Bis(tributyl tin)oxide	biocide treatments / wood preservation?
Lead hydrogen arsenate	biocide treatments / wood preservation?
Triethyl arsenate	biocide treatments / wood preservation?
Benzyl butyl phthalate	softener for PVC

RoHS Review Latest

At the time of writingthere is little new to report about the 46 new proposed substance restrictions. IPC have continued to lobby vigorously and following a formal complaint to the commission that they were excluded from the official review meeting, IPC held their own industry workshop in Brussels which was attended by Commission representatives. The presentations can be downloaded at www.ipc.org/ipcbrussels

The Öko Institut submitted its final report on the RoHS Review during the first week of June. Given that the Commission have a summer break, perhaps something will be available by the time this newsletter is circulated. Any progress should be announced at www.berr.gov.uk/sectors/sustainability/rohs/page29048.html

And finally

I mentioned the Battery & Accumulator Directive in the graphic above. Amongst various restrictions, it will effectively ban Nickel-Cadmium batteries in most applications other than power-tools from the 26th of September 2008. This is another issue for designers: charging circuits for Lithium batteries need to take account of the dangers inherent in overcharging cells using this chemistry.

As I pointed out at the recent ICT Southern Symposium, perhaps the only web link that we need is www.samaritans.org!

Len Pillinger F Inst CT
1st September 2008

A software tool for predicting the thermal performance of embedded components

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Cirflex Technology Ltd.

Abstract

With the growing application of embedded components, the thermal management of printed wiring boards (PWBs) with internal components in addition to conventional surface mounted components is an important consideration. This paper describes the research that has lead to a software tool that predicts the thermal behaviour of embedded passive components in multilayer PWBs. Internal component models are generated using the Transmission Line Matrix (TLM) diffusion method. Individual components can be represented by hundreds of temperature calculation points and are modelled in 3-Dimensions. High resolution board detail is also achieved, with a board typically containing over 100,000 temperature calculation nodes. The software then uses the results from this 3-D data to build up detailed component and board level thermal design rules, delivering accurate results in minutes whilst still maintaining the high detail normally associated with software packages that take several hours to run. The paper also touches on how the software takes into account additional thermal aspects such as board structure, including thickness and position of copper planes in addition to thermal via holes and the other aspects of surface mounts components.

Introduction

The continuing reduction in size of electronic products necessitates a higher packing density of electronic components and the thermal dissipation from these components may become a constraining factor. Furthermore, thermal problems can become more acute if devices are small and embedded within Printed Wiring Boards (PWBs), in addition to being surface mounted. Also, the heat generated by a buried component can critically influence the thermal experience of other nearby components in the same or adjacent layers, possibly leading to premature failure from unduly high temperatures where components are packed too closely together. Clearly, a software tool that can rapidly predict component operating temperatures on the surface of and inside multilayer PWB structures would be valuable in the thermal design process of multi-layer PWBs, and would help to avoid component failure due to component temperature hotspots.

A new software tool (PCBtherm) has been developed by the University of Hull; it has grown from a European collaborative research project. The original research has been further developed to become a highly effective tool for temperature predictions of surface mounted components as well as embedded components in PWB structures. Both relatively simple double sided boards and complex multilayer structures are considered. The structure of the board including layers (wiring and planes), copper & dielectric thickness and thermal via holes are included in the simulation. The results are rapid and enable a 'what if' scenario by changing component positions, multilayer structure of the board and other features.

Simulation Approach

To investigate the effect of embedded component temperature and temperature interaction, a wide variety of multi-layer PWB structures were considered, one of which is shown in Fig. 1.

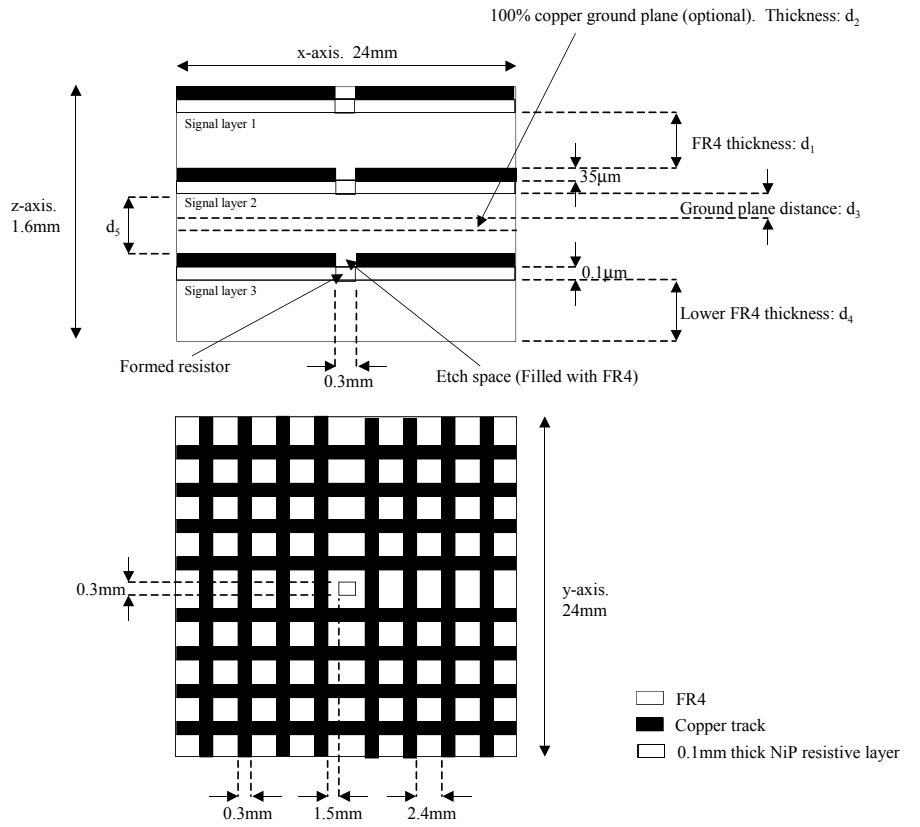

Fig.1 Side and plan view of the simulation PWB structure.

The structure in Fig 1 contains three 0.1µm thick resistive layers made from an NiP alloy, each containing a centered 0.3 x 0.3mm resistor. Immediately above each resistive layer is a 35µm thick copper track layer that has been etched to provide 20% area coverage above each resistive layer. This amount of copper may be typical of a fully populated component layer and the etch pattern that has been used is shown in the plan view. The combination of a resistive layer and copper track layer is termed a "signal layer". Each signal layer is separated from the next by a layer of dielectric (FR4) material. A full cop-

per ground plane at a distance d from layer 2, of varying thickness d_2 is allowed for in the model between signal layers 2 and 3. The remaining parameters d_2, d_4 and d_5 allow for variations in the FR4 thickness between signal layers, and thus allow us to alter the PWB structure in the simulation.

Simulation Method

The simulations make use of the Transmission Line Matrix (TLM) method [8] to solve a 3-dimensional

$$\frac{\delta^2 T}{\delta x^2} + \frac{\delta^2 T}{\delta y^2} + \frac{\delta^2 T}{\delta z^2} = \frac{C_p \rho}{k_\tau} \frac{\delta T}{\delta t}$$

where

k_t ≡ thermal conductivity ($Wm^{-1}K^{-1}$)

C_p ≡ specific heat capacity ($Jkg^{-1}K^{-1}$)

ρ = density (Kg/m^{-3})

The TLM method has been used to solve many diffusion based problems. Examples include prediction of temperature fields in turbine discs, simulation of failure modes in power semiconductor devices, and modelling of thermal effects in glass pressing and ceramic firing [9]. TLM is an iterative technique but, since the diffusion modelling network is unconditionally stable, if the precise transient details are not of interest it is possible to use a timestep such that steady state is reach in a realistic run time. For the purposes of the work presented here, only steady state temperatures are of interest, and we utilise this feature of the model.

An 80 x 80 x 21 size mesh is used to represent the PWB in the TLM model. This results in an in-plane spacial resolution of $\lambda x = \lambda y = 0.3$ mm throughout the whole thickness of the structure. Using this value for λx and λy means that we represent a central resistor of this size using only one node, which in turn means that the simulation can only give us the average temperature of this resistor. The value of λz is varied for each layer type in the PWB. For the 480µm FR4 layers, λz = 96 µm, whilst for the copper layers λz = 35 µm. For the 0.1 µm NiP layers, a λz of 0.1 µm is used.

Heat escapes from the upper and lower surfaces of the PWB via a heat transfer coefficient, which has been initially set to $30Wm^{-2}K^{-1}$. This value is typical for a PWB cooled by forced convection. The sides of the PWB are assumed to be insulated. In the real PWB, some heat will escape from the PWB sides, but this amount will be insignificant when compared to the total heat loss at the upper and lower PWB surfaces. The material thermal properties used in the simulation are summarized in Table 1, from which it is clear that FR4 is thermally orthotropic [4]

	FR4	Copper	NiP
Thermal Conductivity (Wm K)	k=k=1.0 k=0.35	300	5

NiP = Nickel Phosphor Alloy,

FR4 = Epoxy/Glass laminate

Table 1. Material thermal properties

For simulation purposes, the PWB side dimensions are 24 x 24 mm, and the overall thickness is 1.6 mm. This PWB thickness is typical, but the side dimensions are specifically chosen to optimise the model in terms of simulation run time as fully as possible. Though a smaller PWB area for a given level of simulation detail results in a faster running simulation, there is a limit to how small the PWB model can be made without losing generality. If the PWB area in the model is reduced below a certain value, the temperatures inside the board increase because the heat escaping from the surfaces is restricted, [10], and under these circumstances, the simulation results can no longer be considered generally representative of a larger board. To prevent this situation from occurring in the model, it has been found that the simulation PWB size should be at least 24 x 24 mm [10]

Results

(i) Temperature profile and interaction within an embedded resistive layer

A resistor on signal layer 2 in Fig. 1 is set to generate 9mW of power in the simulations. This corresponds to a power density of $100mW/mm^2$. The FR4 thicknesses d_1, d_4 and d_5 are all set to 498µm. The full copper ground plane between signal layers 2 and 3 is not present. Figure 2 shows the in-plane steady-state temperature above ambient within signal layer 2 at various radial distances from the resistor.

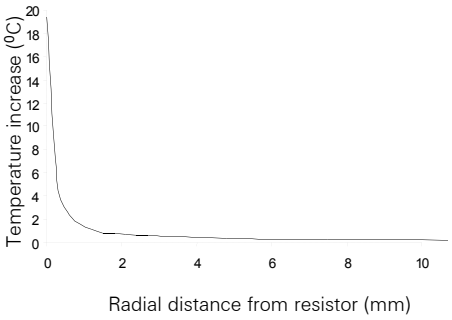

Fig. 2. Temperature profile within signal layer 2.

From the results shown in Fig. 2, the resistor temperature, given by the temperature at x = 0, rises approximately 19ºC above ambient. The temperature then drops off rapidly, and at approximately 2mm from the resistor the temperature is only 1ºC above ambient. In terms of component packing, this means that another component placed 2mm from this one would experience an increase of 1ºC, or approximately 5% of the temperature rise developed as a result of its own operation. This is a small amount, but in a situation where many resistors are placed near each other this increase could accumulate many times over and the increase in temperature could be significant.

To demonstrate the thermal effect of PWB structure, we place a 35µm copper ground plane between signal layers 2 and 3 in Fig. 1 and the distance to the ground plane, parameter d_3 is varied. Fig. 3 shows the in-plane temperature profile caused by a resistor on signal layer 2, again generating 9mw of power, for values of d_3 equal to 250, 125 and 65µm, against distance from the resistor over the first 2mm. We also plot the profile where no ground plane is present, as already shown in Fig. 2, for comparison.

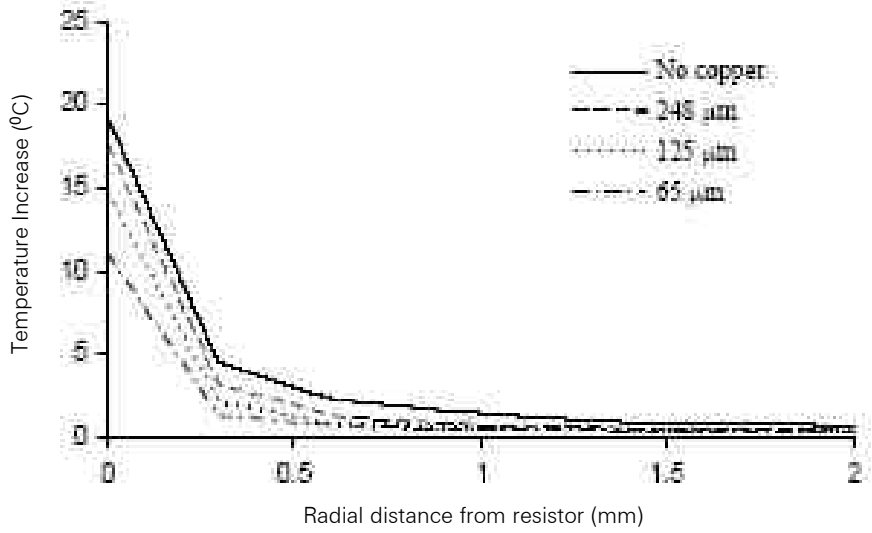

Fig.3 Thermal effect of a full copper ground plane on resistor temperature profile

The results in Fig. 3 show that the addition of a copper ground plane at a distance of 250µm from signal layer 2 causes the resistor temperature to fall from 19ºC to approximately 18ºC. As the copper plane is brought closer to signal layer 2, the resistor temperature continues to fall and is reduced to 11ºC when the ground plane is at distance of 65µm. This reduction is due to the highly conductive path presented by the copper that allows the heat to spread laterally before escaping to the PWB lower surface. It is also evident from the results, that the inclusion of a copper ground plane also improves the potential for high density component packing. The curves in Fig. 3 indicate that when a copper ground plane is placed near signal layer 2, a resistor placed only 1mm away will experience the same 1ºC increase as one placed 2mm away where no ground plane is present. The addition of a copper ground plane therefore not only reduces component temperature, but allows components to be placed more closely together while experiencing the same temperature increase.

(ii) Interaction between signal layers

The number of components that can be fabricated within a given volume of PWB is also governed by the number of layers within it. Clearly, as more layers are added within a given PWB thickness the distance between the layers must decrease, and as this happens average component temperatures are likely to increase As an investigation of this, Fig. 4 shows the steady state temperature profile on signal layer 3 caused by a resistor on signal layer 2 generating 9mW. The profiles are shown for three different distances between signal layer 2 and signal layer 3. This distance is shown as parameter d in Fig. 1, and is altered by varying the thickness of the FR4 layer between layers 2 and 3.

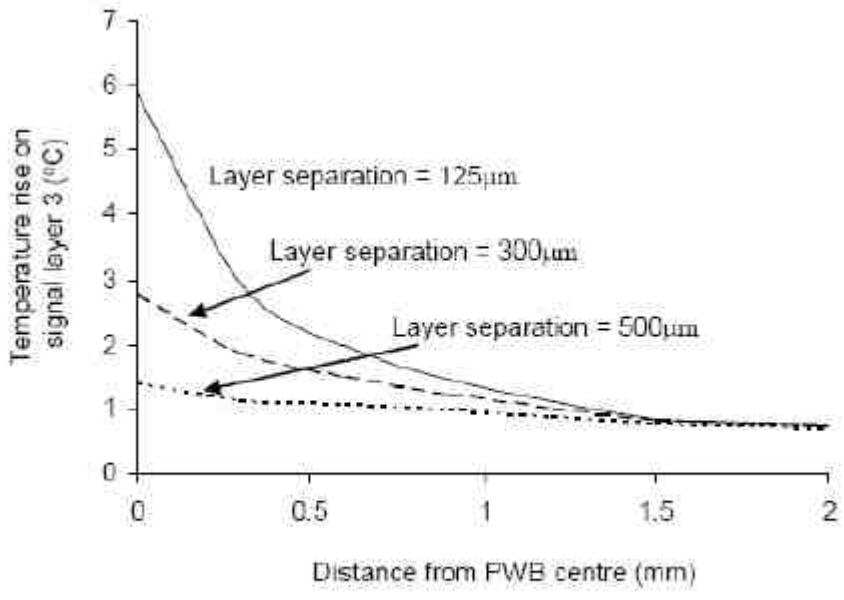

Fig.4 The temperature rise on signal 3 due to a resistor generating 9mw on signal layer 2

The profiles in Fig. 4 show that, as expected, as the distance between the layers is reduced, the temperatures on layer 3 at a point below the resistor increase. The results tell us that if a resistor generating 9mW of heat was placed on signal layer 2, and a second component was placed on signal layer 3 separated by 125 •m of FR4, the component on layer 3 may experience an increase in temperature of as much as 6C as a result of the operation of the component on layer 2. This corresponds to approximately 30% of the temperature rise of the resistor on layer 2.

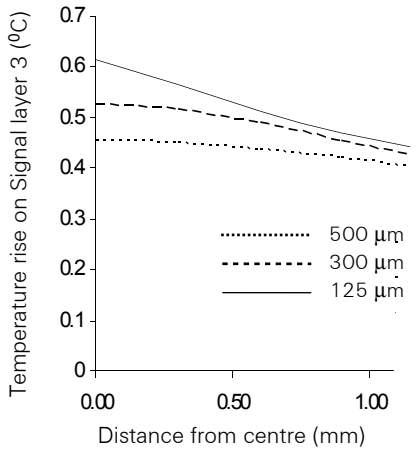

Fig5. The temperature rise on signal layer 3 with 35 mm copper plane

Fig. 5 shows how the inclusion of an embedded 35µm thick copper ground plane placed halfway between signal layers 2 and 3 affects the thermal interaction between the layers. Again, the profiles for three different layer separations, 500, 300 and 125µm are shown.

The results in figure 5 show that the inclusion of a 35µm copper plane in between signal layers 2 and 3 has reduced the maximum temperature on signal layer 3. In fact, at a layer separation of 125µm, the inclusion of a 35µm copper plane reduces the maximum temperature on signal layer 3 from approximately 6ºC, as shown in figure 5, to 0.6ºC. This reduction in temperature is again due to the high thermal conductivity of the copper, which acts to spreads the heat laterally before it reaches signal layer 3. The inclusion of such a copper plane will therefore also allow closer packing of signal layers and thus enable more components to be fabricated within a given thickness of PWB.

(iii) Effects of resistor area

The relationship between the area of an embedded resistor and its temperature has been investigated by Blanco and Mansingh [1]. They measure the temperature of buried resistors of different areas and obtain an analytical equation that closely matches experimental results. The expression derived by Blanco and Mansingh is

$$T = \frac{0.377P}{A^{0.396}}$$

where T is the temperature in C, A is the area of the resistor in mm, and P is the bulk power applied to the resistor in mW. The PWB structure that Blanco and Mansingh use is shown in Fig. 6. The structure contains a single buried resistive layer with a copper track layer directly above it, and one full copper plane.

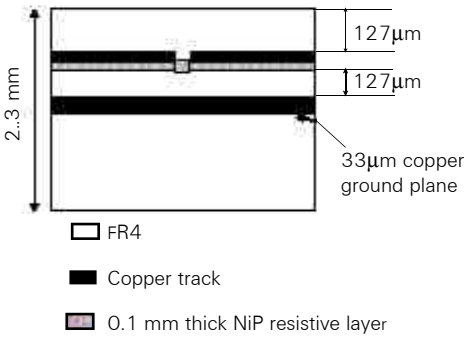

Fig.6 PWB structure used in reference [1]

The results presented in this paper are for a 0.3 x 0.3mm resistor. However, it is possible to obtain the temperature of larger resistors by the use of superposition. If we take a temperature profile such as that shown in figure 3 for a copper plane separation of 125µm, and rotate it in its plane by and angle 360º, we obtain a profile of the temperature over a circular area within the signal layer. We can then consider this as a thermal footprint for a 0.3 x 0.3mm resistor. Now because the temperatures are steady state, we can superimpose such a thermal footprint upon another to obtain an approximate combined steady state thermal footprint. This is only an approximation because when we superimpose the thermal footprint caused by two or more different resistors, their positions relative to the copper track in the resulting thermal footprint will be different and, therefore, we are not superimposing the footprints within identical scenes. However, because the copper track is quite far away from the resistor, its overall effect is small, and the resulting superimposed footprint can be considered to see a typical amount of copper within the layer. As well as the copper, the effect of the NiP material on the thermal background for superposition must also be considered. However, this is negligible, because the NiP material is so thin (0.1µm) when compared to the 35µm FR4, and a resistor sees another resistor within the thermal background as FR4. It is therefore acceptable to use a superposition approach to obtain the thermal footprint for a large resistor from the thermal footprint of a 0.3 x 0.3mm resistor. For example, if we wished to obtain the thermal footprint for a 0.6 x 0.6mm resistor, we could do so by superimposing four translated versions of the thermal footprints caused by a 0.3 x 0.3mm, and scaling them accordingly. This process can be applied to any thin film resistor that has dimensions which are, in our case, integer multiples of 0.3mm, and we now use this process of superposition to compare our simulated results with those predicted by equation[1]

Fast Prediction of Temperatures

To simulate every different PWB configuration using a computer model would be a long and tedious process, as each simulation can take many hours, or in complex models, as much as several days. For a one-off simulation, this may be acceptable, but as a design tool it almost certainly is not. However, there is an alternative approach. By simulating a very wide range of different PWB structures, it is possible to build up a substantial database of steady-state results. Interpolation techniques can be applied to these results to make predictions on steady-state component temperatures in PWB structures that fall inside the range of simulations. Furthermore, to account for different component positions and geometries, results can be rotated, translated and superimposed upon each other to build up a complete thermal map encompassing the thermal interaction of many components within a single layer [2]. By systematically applying this process, a complete picture of the temperatures inside many different multi-layer PWB structures can be built up. Furthermore, this approach is relatively quick, and results can be obtained in just one or two minutes, even in the most complex of cases. The database was produced through empirical results as is the verification of the simulation.

To demonstrate this approach and as a means of validating the profiles

already shown, Fig. 7 compares the temperature rises predicted by equation[1] and those predicted by our simulations for square resistors of areas ranging from 0.09mm² to 9mm² in a PWB whose structure is shown in Fig. 6. The resistor is set to generate 20mW of power. The simulation results for each resistor size were obtained by superimposing and scaling the temperature profiles produced by a 0.3 x 0.3mm resistor placed on the signal layer in Fig. 6.

The simulation results agree extremely well with the predicted results. The method of superimposing results based only on a small resistor to obtain the temperatures of much larger resistors is very efficient. It means that from a set of results based on one resistor size we can obtain information about larger resistors.

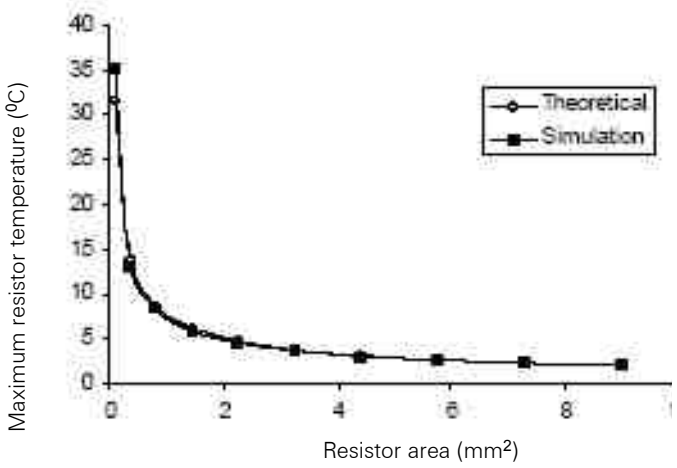

Fig.7 Variation of resistor temperature against area.

Software Output

All of the simulation results presented here, plus others based on various PWB structures have been combined and entered into a piece of software. The software makes use of the linear superposition process, as already mentioned, to predict the temperatures caused by many heat generating thin film resistors of different sizes inside a multi-layer PWB. As well as predicting the tempertures casued by thin film resistors, this software is also capable of modelling other surface mount component types such as Ball Grid Array (BGA) packages, Quad Flat Pack (QFP) packages and others.

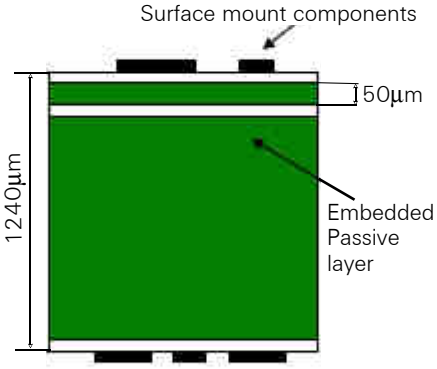

Fig.9 3 - layer PWB structure

The structure shown in Fig. 9 contains 1 internal signal layer containing embedded resistors. Various components are situated on both sides of the structure. Figure 10 shows an initial GUI of the software tool that has now been developed. CAD data has been loaded into the software through the IDF data format. This provides information on the board dimensions and component types and positions on the outer layers; internal layers are added separately to build up the structure of the board, including internal layers with embedded resistors.

Fig. 10 shows a plan view of the top layer of the 3-layer board and a cross-section view. The structure of the board is fully editable through the cross-section window, including dielectric separations, wiring and copper planes of various copper thicknesses.

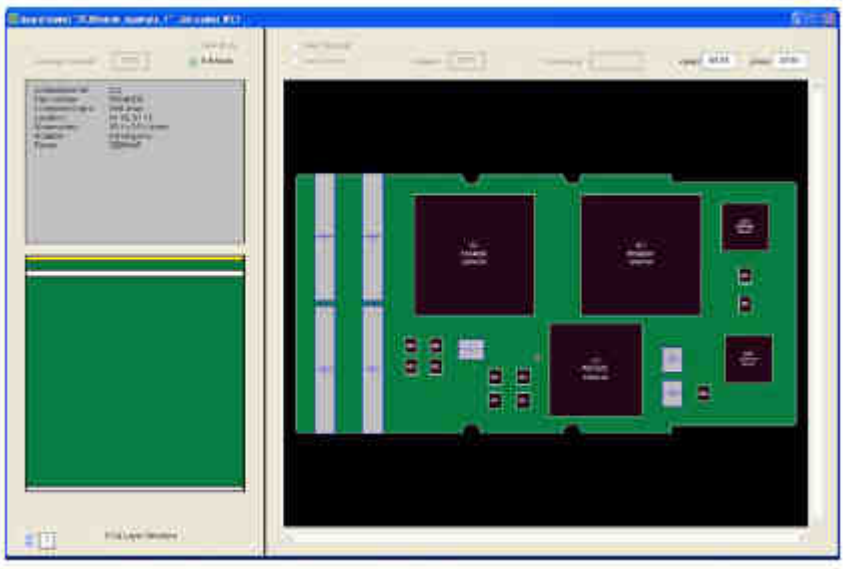

Figure 10. Initial view of PCB structure in the software

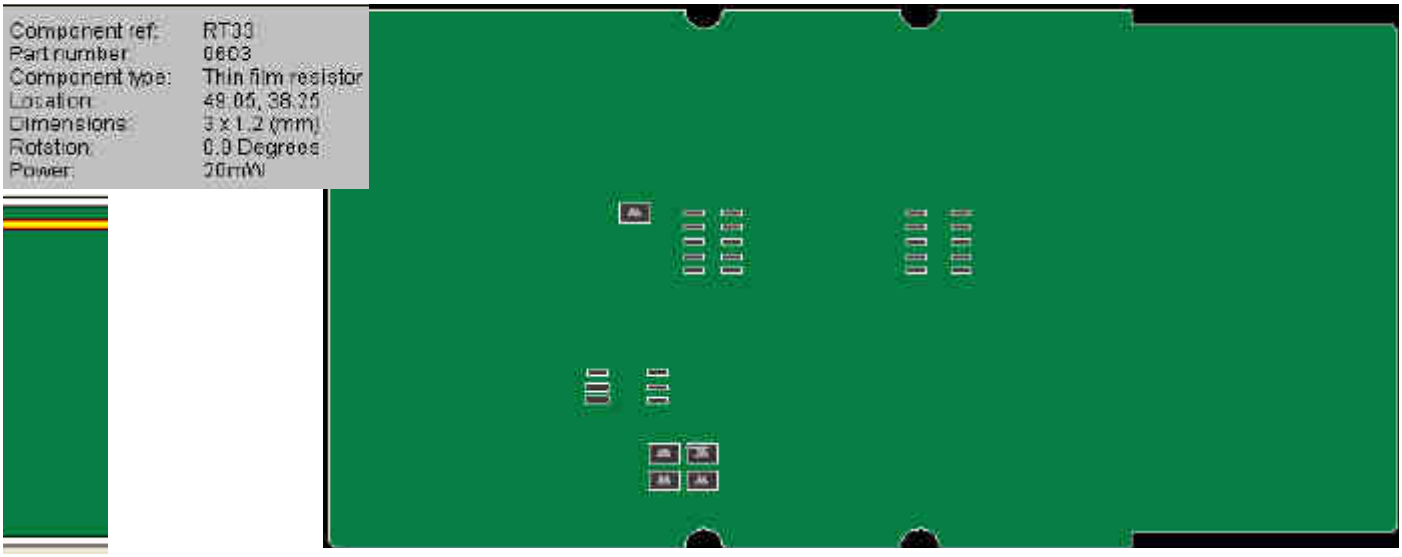

Figure 11 shows a plan view of the thin film resistor layout on the embedded layer.

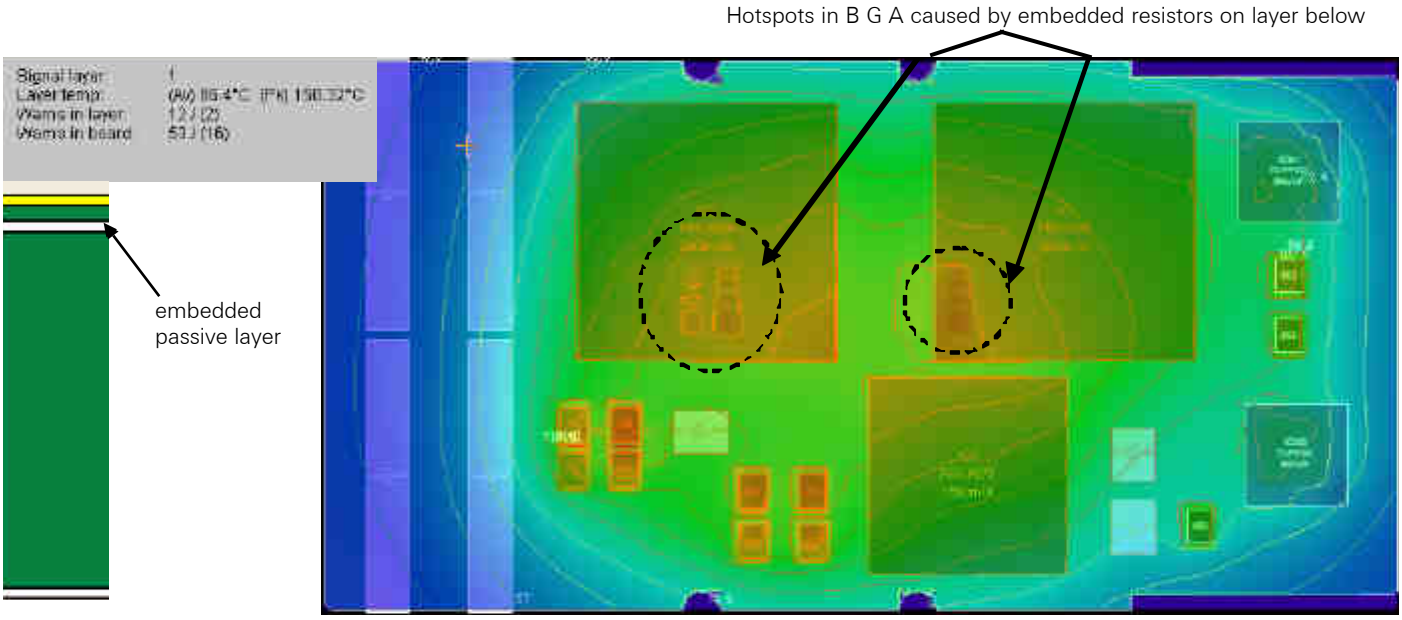

Fig 12. GUI showing simulated temperature profiles on the upper PWB layer in two areas in the BGA devices where the embedded resistors are causing hotspots in both of the surface mount BGA devices. The software indicates that these hotspots are approximately 110 .C above ambient.

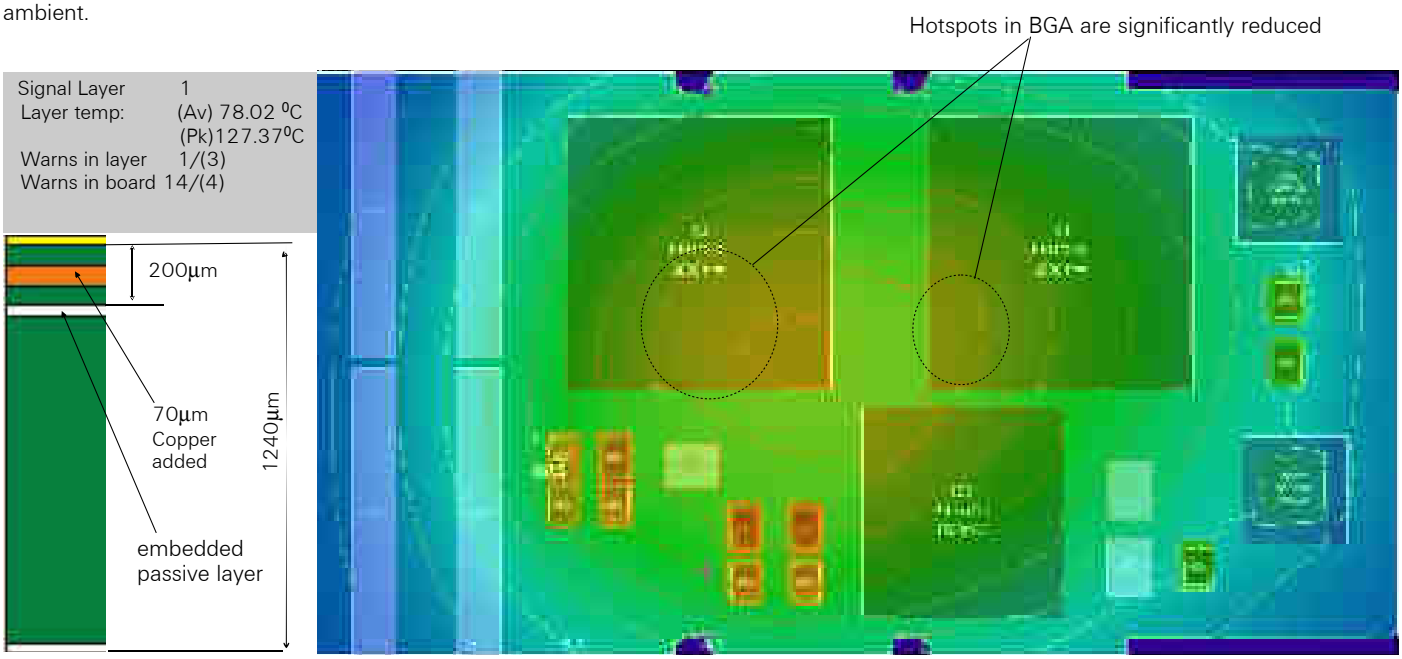

Fig. 13 70mm full copper plane

Fig.14 Simulated result after modifying structure according to diagnosis of Fig.12

Conclusion.

A detailed study of the effects of board structure on the temperature of embedded resistors has been completed. A software tool has been developed which uses these results to make rapid predictions of component temperatures inside complex multi-layer PWBs, containing both embedded and surface mount components. Design data can be imported and all the important features of a PWB can be accommodated including board structure, embedded component position, the position and thickness of copper ground planes and PWB buildup. The software enables a 'What If' scenarios to be run, and changes can be exported back to a CAD system should this be required.

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EMI Shielding Properties of Polymer Composites

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Introduction

Shielding from radiated electromagnetic interference is a constantly growing issue with the increase and miniaturisation of electronic devices. Often these devices require shielding from the external EM environment or from internally generated sources such as self generated waves or from adjacent circuits. Considering this EMI issue while designing of a PCB will aid the overall efficiency of the process as it is a common scenario that "decisions on the RFI enclosures are left until the end of the design process creating a situation that makes their addition more difficult to accommodate. As a result, the enclosures may interfere mechanically with other areas of the design."(Warner, 2008). Considering available shielding options at the design stage will help to control the cost, manufacture and weight issues while also potentially expanding the options available for the desired application.

Shielding methods

The majority of unwanted EM emissions are the result of voltages and currents travelling within circuitry, where voltages generate electric fields and the currents generate magnetic fields. Good design and grounding can reduce the levels of these emissions but often it is necessary to provide a barrier shield. Just as conductive materials will emit radiation they also reflect and absorb it converting it back to voltages and currents.

Board level enclosures are one of the standard methods of shielding within PCBs and circuitry, they are housings that surround the component providing it with a conductive cage to shield and reduce the levels of emissions entering or being transmitted from the device. Enclosure design is varied but in general they take the form of a conductive blanket known as a "shadow shield" or a five sided box that encapsulated the desired components, they can be multi cavity and have accessibility for maintenance via hinged flaps. Commonly these are thin metallic sheets that could be stamped, folded or machined to shape, the manufacturing process followed will depend on the volume required and the stage of development reached. Metallic shields perform well when manufactured and installed correctly but there is a risk that further processing of the board can result in apertures being created, if these are of similar length to any wavelengths involved, they can act as an antenna for localised emissions.

Polymer enclosures are a viable option in terms of cost weight and manufacturability but with most commodity plastics being excellent insulators they are essentially invisible to EM waves. Therefore to utilise polymers they have to include a conduction mechanism, this could be in the form of metallisation, doping, inherent conduction or conductively filled polymers.

Metallised plastic housings involve depositing a very thin layer of metal onto a moulded plastic enclosure providing a continuous conductive path that can provide high EM attenuation levels. Possible metallisation processes include :-

a) **Electroless plating** – A chemical reduction process that requires various stages of baths to sensitise and activate the surface of the material before finally being submerged in a solution rich in metal ions that are deposited uniformly over the all active surfaces. This provides a two layer shield as both internal and external surfaces are coated resulting in a potential shielding effectiveness in the range of 90dB (Bastenbeck, 2008). Although a good method of providing shielding this requires large amounts of chemicals and can have slow deposition rates.

b) **Vacuum metallisation** – Various vacuum plating process are feasible, these include evaporation coating where a metal is vaporised then deposited onto the substrate surface and sputtering where by the introduction of a current and inert gas within the vacuum chamber creates a plasma which releases metal atoms from a target material which are then deposited throughout the chamber. These processes are relatively simple and provide good quality coatings but are limited by the chamber dimensions and are both line of sight processes making complex substrates more difficult to coat. They can achieve shielding in the region of 50-70dB (Gerke, 1990) depending on the frequency and thickness of the coating, at lower frequency the coating must be thicker to compensate for the skin effect.

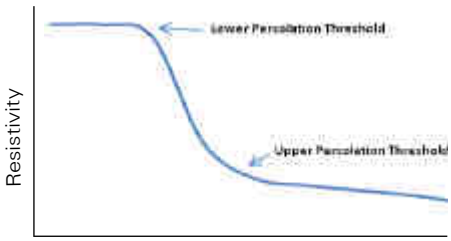
Inherently conductive Polymers

Polymers that are conductive as a property of their structure are known as inherently conductive polymers (ICP), they can be synthesised for a specific structure or to contain dopants to allow electron transfer. One solution can be achieved through modification to the polymer structure to allow the transfer of electrons along a chain structure know as a conjugated chain polymer. These involve chemically unsaturated polymers that have a back bone chain structure of alternating single and double bonded carbon atoms. This structure allows for each carbon atom to only be bonded with one other kind of atom this leaves one electron free from each carbon atom and allows for electron transport within. Although ICP's are potentially ideal for these applications often their high crystallinity and insolubility have limited their use, although more recent developments have shown more promise.

Conductively filled polymer

Conductive polymer composite are manufactured by filling an insulative matrix with conductive fillers, the matrix gradually becomes less resistive as the volume of filler increases. This trend continues until the filler volume reaches a level where the resistance rapidly drops known as percolation threshold, this resistance drop continues until a limit is reached and the reduction in resistance slows down again. At this stage conductive networks have been formed and once percolation has been reached the addition of further fillers is unlikely to give any significant improvement to the conductivity but maybe likely to have a detrimental impact on the mechanical properties of the composite.

Typical Percolation Curve



Conductive Filler Volume (%)

Percolation threshold values are varied dependant on filler and matrix properties and with the filler usually the heaviest and most costly aspect to a composite, reduction in the percolation threshold value will reduce amounts of filler required. Common fillers include metallic or carbon powders, flakes or fibres and also ICP particles dispersed into a non conducting matrix are being researched.

Polymer composite manufacture

Samples were manufactured in a matrix of poly(methyl methacrylate) PMMA resin and using commercially available filler materials such as nickels, graphite's and silver coated glass. These are then printed following a simple hand mixing and automated printing process. Hand mixing is preferred to mechanical or ultrasonic mixing as the more dispersed the particles the more likely they are to be isolated within the insulative matrix and therefore less likely to form the desired conductive networks. The samples are then printed on a K-control coater, where a wire wound bar is drawn down the substrate giving a uniform coating at controlled thicknesses, then cured inside an oven at 80ºC.

Filler Materials

The range of filler materials tested covers the commonly used types of conductive particles used for these types of applications they are;

Expanded Graphite

Expanded graphite is a form of graphite powder that has been chemically and heat treated to increase its volume giving a very low density conductive powder, measured at 0.098 g/cm^3 It is formed by taking natural flake graphite and treating it with acids then rapidly heating it to temperatures in the region of 1000^0 C (Figure 1). This process expands the weaker interlayer van der Waals bonds which then allow the individual layers to collapse and support their surroundings allowing for the expansion to remain after cooling. This process can expand the graphite to between 100-300% of its volume therefore should allow for low percolation values and lightweight composites.

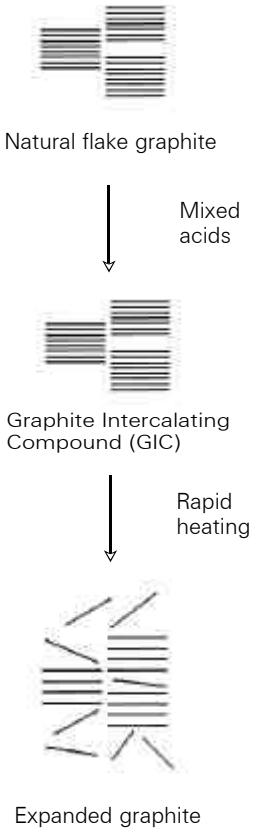
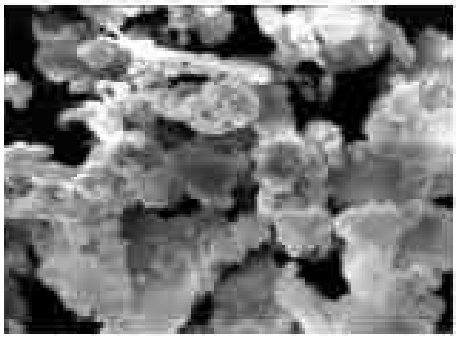
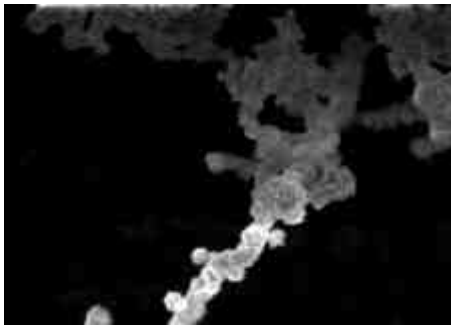


Fig 1.Formation of Expanded Graphite (Zheng)



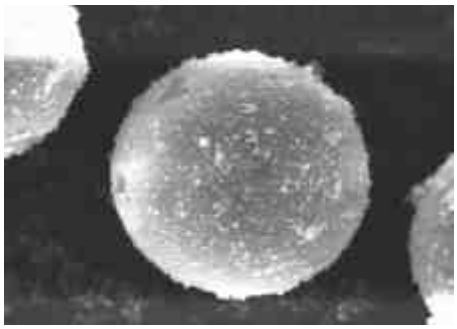
Flake Nickel

Flake nickel is a powder with a high aspect ratio of close to 20 to 1 allowing maximum area of contact between the particles and therefore reducing the contact resistance.



Filamentary Nickel

Filamentary nickel is a fine powder that has been produced through heat treated nickel carbonyl giving filamentary, type particles that should form networks more easily within the matrix.



Silver Coated Glass

Silver coated glass spheres have the advantage of combining the lightweight glass core with the excellent electrical properties of the silver coating. Silver is one of the most conductive materials and also has a conductive oxide therefore degradation of these materials isn't as drastic as with other metallic powders,

copper for example can require an acidic additive to inhibit this effect

Resistivity Measurements

Surface resistivity is a material property describing the electrical resistance of a set area of the materials surface, it is measured following the parallel plate electrode configuration described in the standard ASTM D257, and this involves measuring the resistance between two parallel copper electrodes over a known square area. The potential applications for conductive materials are predominantly determined by the level of resistivity achieved, as can be seen in figure 2 materials that are less resistive than plastics are capable of dissipating static charges and materials close to the resistivity of metals have far greater shielding properties.

Attenuation Measurements

Attenuation measurements were taken on a Rohde & Schwarz ZVA network analyser using a waveguide with a range 2.6GHz – 3.95GHz. Samples of the printed materials were placed in between the two halves of the waveguide and the through transmission attenuation due to the coating material was measured. Calibration was performed with a blank polyester sheet substrate therefore the attenuations evaluated were of the coatings only.

Results

As can be seen in figure 3, all materials followed the classical percolation behaviour with the resistivities dropping rapidly between 35-45% with the exception of the silver coated glass which occurred slightly higher at about 50-55%. The raised level may be due to the spherical nature of the particles having less contact area available, although when percolation occurred the resistivity dropped dramatically. The expanded graphite shows the limitations of carbon based fillers, with graphite being inherently more resistive even after percolation it was far higher that the other materials. Both the nickel samples followed almost identical curves reaching ohmic levels after about 40% volume.

The attenuation measurements shown in figure 4 were measured from the point of each materials upper percolation threshold and shows a significant increase in shielding effectivness with the silver coated glass sample although readings were taken at 55% volume it was measured to have a similar resistivity as the nickel samples yet achieved around a 20dB increase in shielding. The expanded graphite sample provided very little shielding and is only

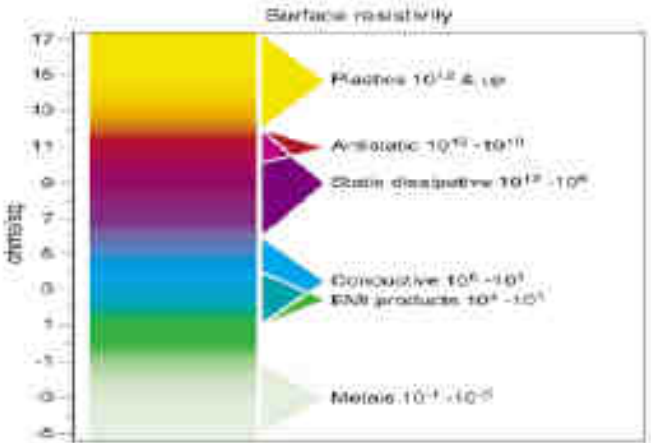


Fig.2 Surface Resistivity Applications (RTP Company)

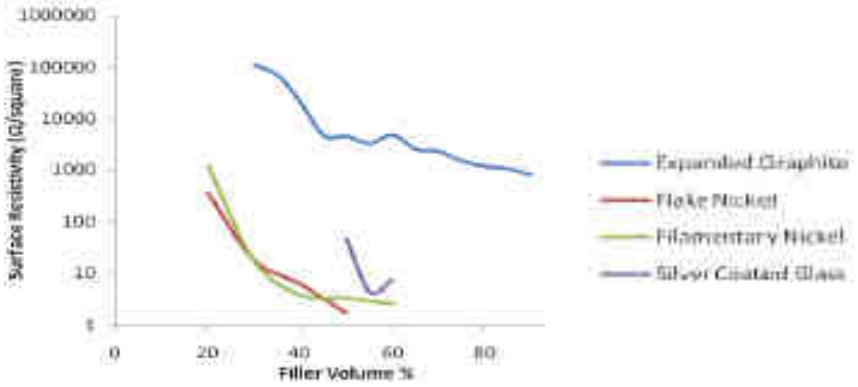


Fig.3 Resistivity Measurements

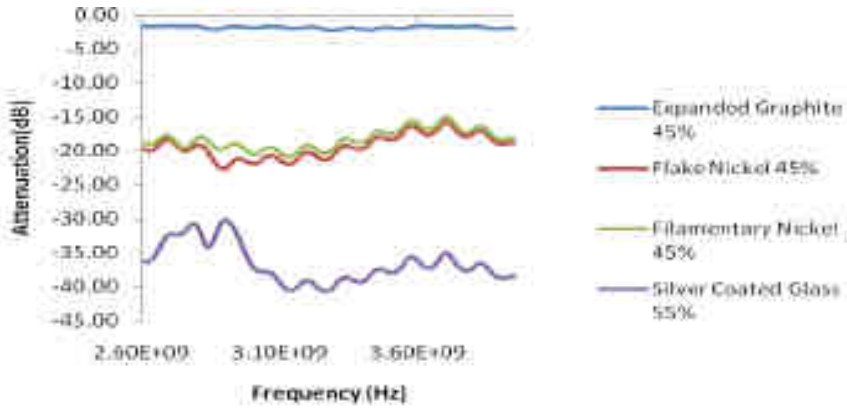


Fig.4 Attenuation Measurements

Conclusion

Although conductive polymer composites can be benificial interms of cost, ease of manufacture and weight saving benifits the limitations of the shielding effectiveness restrict their potential applications . Efforts will continue to be directed towards developing these materials with a goal of increasing the conductivity and shieding effectiveness while keeping the metal content to a minimum.

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PCB Solderability Changes with Time – What Finish is Best?

Bob Willis ASKbobwillis.com

"When you evaluate any PCB surface finish you must consider the reality of real world production processes. Although printed boards and components go into your process, ideally they come out the other end of the production line, however there can be many stops along the way".

Circuits boards can be subjected to many of the following steps during manufacture, each step may impact the solderability of the surface finish. If solder levelled boards are used, either tin/lead or lead-free and the thickness of the coating is maintained there is limited impact. Tin, copper, silver and gold will see a change in the degree of wetting.

Baking boards
PCB pre wash
Multiple reflows
In process cleaning or wash off
Adhesive curing
Reform then wave or selective soldering

Sample boards previously subjected to one or two reflow cycles were tested 10 days after the first reflow using a MUST 2 wetting balance. The following graphs show the changes in solderability after one reflow operation; the results are exaggerated due to the hold time prior to testing. However it is well known that some alternative surface finishes do not hold up to one reflow cycle and extended hold time before the second soldering operation. This is a critical issue when selecting surface finishes. Some companies build their products or contract out the assembly and only complete the final assembly when orders are received. There are many delays that can occur in the manufacturing process, some are unavoidable some are actually planned but not considered during a surface finishes evaluation phase.

Test conditions used on the wetting balance

Solderability testing conducted with 200mg SAC pellet

One pellet per test site, pellet change during multiple testing

Temperature set point 260C
No hold for pre-heat
Speed 0.1mm/second
Flux ACTIEC5

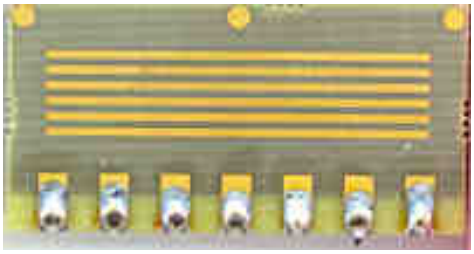


Fig 1 Close up of gold test coupon used on the wetting balance, the pads shown have previously been tested. The parallel lines also seen on the sample are used for solder paste dot spread test for shop floor in production evaluations.

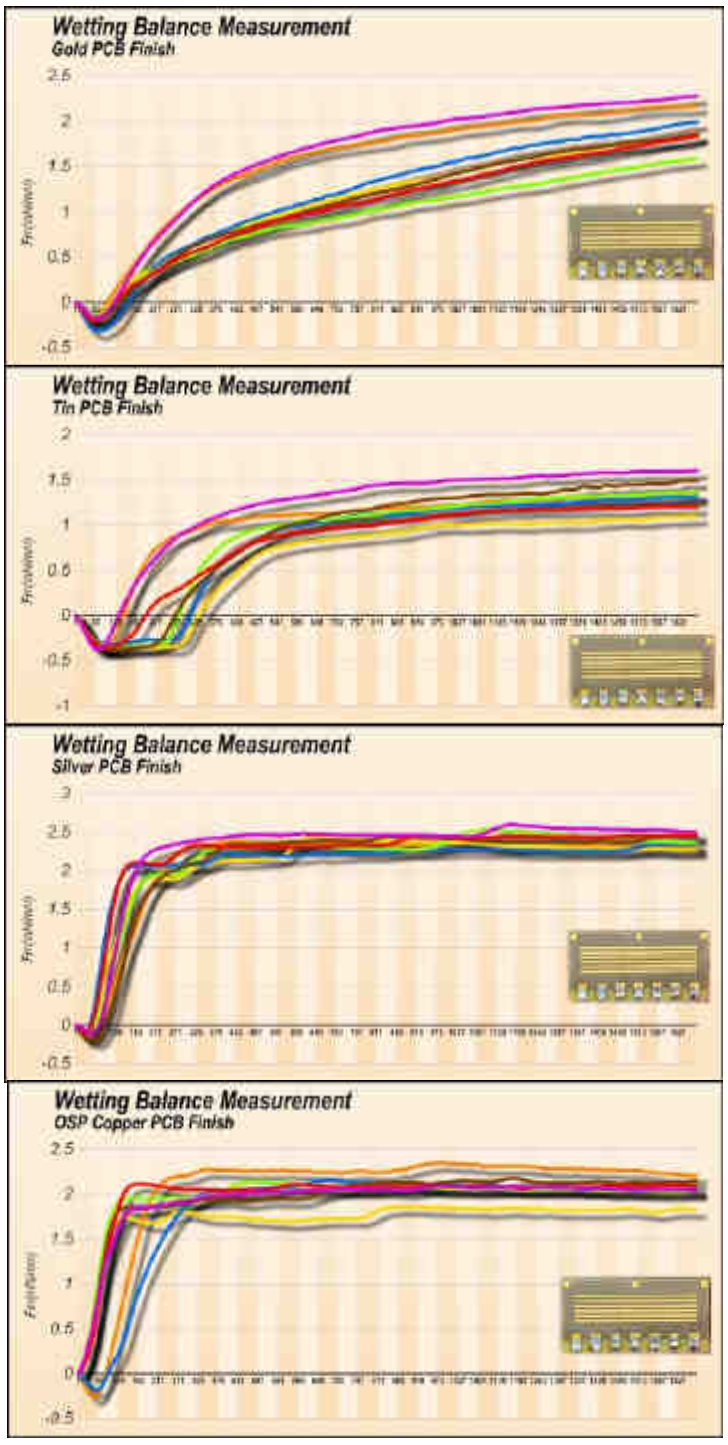
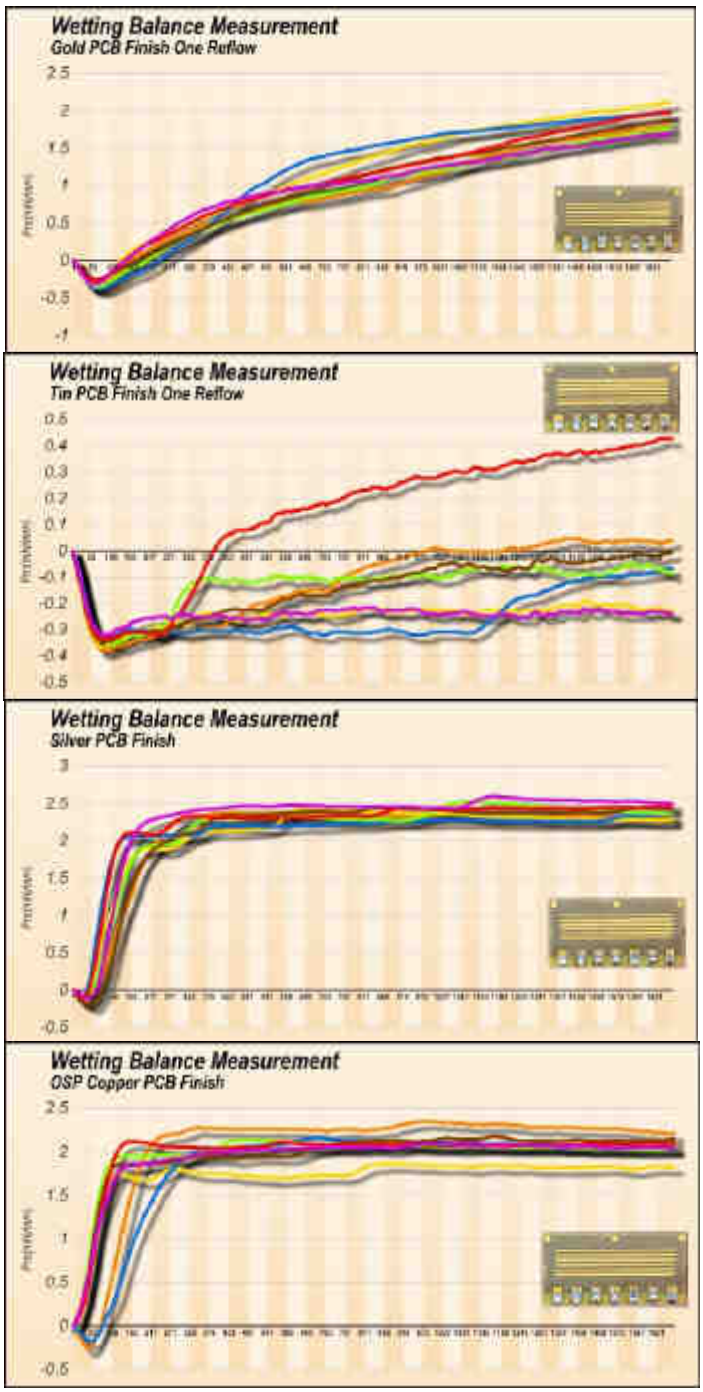


Figure 2, 3, 4, 5 graphs show wetting balance measurements for gold, tin, silver and Copper OSP prior to reflow soldering.



The second group of wetting balance graphs figure 6,7,8 and 9 show the change in performance after one reflow cycle and a hold of 10 days in an ambient condition waiting for second stage assembly.

Rotary Dip and solder float solderability test methods are used by the printed board industry, but are very limited and basically the same as the dip and inspect test used for surface mount components. It is very difficult to demonstrate the subtle changes which take place on boards as they are subjected to multiple heating operations during the manufacture or assembly. To provide repeatable results the wetting balance may be used to assess changes in solderability on test pads, audit panels or even pre-production boards.

Using these techniques assembly companies and printed board manufacturers can use the wetting balance to guarantee the solderability of boards and components in their drive for zero defect manufacture. The test has often been used by the author for material evaluations, the impact on assembly process stages, the change in flux activity and supplier audits. It is also a useful technique as part of product development or to provide customers with technical support. Use of this test method eliminates the arguments which often arise whenthe soldering quality does not provide the expected soldering yieldsinproduction.

Further information on the solderability test equipment and testing services can be obtained at www.gen3systems.com/index.php

Bob Willis is a process engineer providing engineering support in conventional and surface mount assembly processes. He runs special production features at exhibitions and also offers his seminars and workshops worldwide. These complement his own practical in hose hands on workshops. For further information on how Bob may be able to support your staff with **on line consultancy, in house training go to**

www.ASKbobwillis.com

34thAnnual Symposium of the Institute of Circuit Technology, 3rd June 2008

Institute of Circuit Technology Chairman **Steve Payne** welcomed delegates to the 34th ICT Annual Symposium at Tweed Horizons in the Scottish borders, and reflected upon the early years of the Institute, in an era before the introduction of personal computers, mobile phones and the Internet, when the Institute was the lleading body in the industry and was a founder member of the Printed Circuit World Convention. Although numbers had declined as the industry regressed in the late 1990s and early 2000s, membership had continued to grow steadily throughout the last 12 months and now stood at approximately 230.

An encouraging demographic was that the Institute is getting "younger" in terms of average age of members. Payne was confident that the UK would continue to play an important role in the innovation, design and fabrication of printed circuit boards from flexible circuits to the most complex multilayer structures, and emerging technologies such as printed electronics.

The keynote address came from **Dr Peter Hughes OBE,** Chief Executive of Scottish Engineering and leading spokesman on matters affecting the Scottish manufacturing engineering sector. His infectious enthusiasm for the opportunities that exist in industry in Scotland was evident from the outset.

With clearly presented statistics he reminded the audience just how significant was the Scottish manufacturing industry and its contribution to exports. It was enlightening to learn that electronics is bigger business than whisky!

But the key to the future success of industry lay in education and encouragement of young people. In recent years an "obsession with qualifications" had led to a disparity between what Scottish employers needed and what education and skills training youngsters could access.

A university education was not an essential; the actual requirement was for a system for developing skills that met everyone's objectives and equipped individuals with abilities flexible enough to meet the needs of today and respond to the demands of tomorrow.

Many routes were available for young people to fulfil their potential, the strategic expansion of apprenticeship being a practical means of filling the skills gap amongst Scotland's future workforce. Not many keynote speakers include a surprise musical feature. Dr Hughes, with the help of some audience participation, rounded off his presentation with a demonstration of his skills on guitar, mandolin, autoharp - even the McNally Strumstick!

Data management in electronic design and manufacture was the topic discussed by **Carl O'Roche** of **Quantum CAD**.

In a competitive industry where the differentiation between best-in-class SMEs and average companies was their success in meeting product development objectives and consequently driving profitability by driving product to market.

Collaboration was of utmost importance, particularly in a context of increasing outsourcing of activities and increasing numbers of external partners.

The control of product realisation and project management in the development and engineering phase was becoming increasingly difficult, with numerous modifications, revisions and product versions and the increasing stream of communication involved. In the specific example of a design bureau acting as an external partner, efficient control of data was crucial.

O'Roche described how Quantum had adopted a proprietary dynamic data management system as their collaboration platform for controlling and tracking all of their PCB data. It was a flexible web-based server/client system with full project flow control and event logging. All files were securely stored on their server, with nothing left on susceptible file systems, and everyone involved in the project had their own username and password to log on to the server and access their design data in a central shared area.

Every visit was recorded and notification alerts were sent automatically to inform users of changes to a file.

All previous versions of drawings and documents were retained. The system had shown measurable benefits in visibility of changes and verifying completion of changes. O'Roche's comment that "20% of your time every day is spent looking for documents" provoked a unanimous murmur of agreement from members of the audience.

Jonathan Smuga from **Napier University** reported the progress of a project to develop **conductive polymer composites for EMI shielding applications,** being conducted in collaboration with an industrial partner specialising in the manufacture of pigments, metal powders and metal flakes. (*see p. 12- 14*)

Having explained the basic mechanism by which voltages and currents in a device can induce corresponding voltages and currents in a neighbouring device, he discussed the theory of shielding and the factors determining whether electromagnetic radiation was transmitted, absorbed or reflected by the shielding material.

A significant parameter was the intrinsic impedance of a surface, a ratio of the electric to magnetic field amplitudes, which decreased with increasing conductivity.

Of the options available for creating an EMI shield, solid metal enclosures were prohibitively expensive for most applications and plastics offered a more cost-effective solution provided they could be made sufficiently conductive.

Thermal metal spraying gave only line-of-sight coverage and could cause degradation of the plastic surface. Electroless copper plating could give uniform coverage but involve a relatively slow multistage wet process. Vacuum deposition and sputter coating techniques had the limitation of chamber size, and applied metal foils were too labour intensive for other than prototypes.

Having discounted these options, attention was focused on conductive plastic composites, which offered the potential to combine metallic conductivity with plastic processability.

Conductive fillers were judged to be a more practicable choice than inherently conductive polymers, charge transfer complexes or organometallic compounds. Candidate materials were filament nickel, flake nickel and expanded graphite, added to the "percolation threshold", at which the material becomes conductive.

Coating formulations were prepared by dispersing the fillers in solvent to prevent agglomeration, then blending them into polymethyl methacrylate resin. Samples were coated and dried then measured for surface resistivity, EMI attenuation and reflectivity.

The resistance values of the graphite-filled samples were too high for the

material to be effective as an EMI shield. The nickel-filled examples showed gave more encouraging results. Future work would include testing at higher frequencies – up to 40 GHz, and modelling with Comsol Multiphysics software.

Alan Colquhoun, Principal DfM Engineer at BAE Systems Hillend, presented a **worked example in design for manufacture.**

He demonstrated what could be achieved by a DfM/DfT integrated project team in improving the manufacturability and testability of a design.

The engineering methodology facilitated the design of products such that they were easy to manufacture. General objectives were:-

a) to reduce the number of parts to minimize the opportunity for a defective part or an assembly error
b) to reduce the total cost of fabricating and assembling the product,
c) to design verifiability into the product to provide a natural test or inspection of the item,
d) to avoid tolerances beyond the natural capability of the manufacturing processes,
e) to design for ease of assembly by minimizing fastenings and hand-soldered joints,
e) and to design for ease of servicing the product.

The DfM/DfT team also made the effort to understand more about the capabilities and limitations of the production system, in order to refine design rules to further guide and optimise the product for production.

Colquhoun used a hypothetical assembly to demonstrate how, with logical reasoning in a team environment a stage-by-stage cost reduction of 30% could be achieved.

In the real example of the Commander radar system, a total saving per system of £200,000, at a cost of 21 man days work, had been made by his DfM/DfT integrated project team.

In a presentation entitled **Fine lines with LDI, Uwe Altmann** from **Orbotech** began with the question: **What do you mean by fine lines?**

Many manufacturers would refer to their own capability and answer maybe 100 microns or 75 microns. Orbotech defined "fine lines" as 50 microns and below, and already had the machine capability to achieve 15 microns, although developments in photoresist capability were awaited before these dimensions could be realised in production.

He listed the benefits of laser direct imaging, "photolithography without a mask", as the elimination of repeat defects and vacuum-contact effects, and the minimisation of surface topography effects by the +/- 300 micron depth of focus of their Large Scan Optics, which had been developed in collaboration with Zeiss in Jena.

He explained in detail how the optical system had a total beam path of 9 metres, with the laser being transformed into multiple beams and reflected on to the panel by a rotating polygon mirror. Each pixel was independently addressable, and the on-the-fly dynamic-scaling system could achieve registration to +/- 12 microns, with compensation for panel orientation, and dimensional distortion.

Typical throughput was 80 double-sided panels per hour, using an 8-watt laser and a resist of 10-16 millijoule photospeed.

Altmann demonstrated the precision of the system with photographs of a pattern of 25 micron lines in a dry film 100 microns thick, which showed extremely cleanly defined vertical sidewalls.

Additional features of the LDI system were its ability to mark panels with individual serial numbers, date and scale-factor stamps and bar codes.

Francesca Stern of BPA achieved a breakthrough in communications technology, with the Institute's first-ever remote presentation. Her PowerPoint was in the conference room, her voice was in the conference room, but Francesca herself was in BPA's office, nearly 400 miles away.

She explained in detail how BPA went about their business of analysing and forecasting business information and producing technology roadmaps.

She used the analogy of driving a car: the driver needs to see very clearly where he's going, whilst at the same time knowing what's going on around him, and he needs to know critically when, and which way, to turn - forecasting helps the driver make that decision.

Forecasting was all about accumulating data from the past and intelligently extrapolating it into the future. Francesca demonstrated the various ways in which growth curves could be presented, and techniques for smoothing the curve so that underlying trends became more clearly visible.

She discussed the use of "leading indicators", economic indicators that change before the economy has changed, such as average weekly hours worked by manufacturing workers, new housing starts, unemployment figures, money supply, inventory changes, new orders for capital goods and stock exchange prices.

But these were only useful for short-term forecasting. National statistics, input from trade associations, response to questionnaires from companies in the industry – all contributed to the information from which forecasts were prepared.

Factors like international conflicts, currency effects and national disasters could all push data out of shape. With few exceptions, history showed that BPA's forecasting had been consistently accurate, and the forecast continued to operate as tools to highlight trends and turning points so that executives could swing the steering wheel in the right direction at the right time, and know when to tread on the accelerator or the brakes.

The final presentation came from **Mike Osmond of Intrasys Design,** on the subject of **"Maintaining the Balance",** with reference to DfM, or, as he put it, DfX - design for all desirable attributes or, more simply, design for excellence.

PCB design was a physical definition of the electrical requirements – a transition from concept to the real world. But in today's real world it was no longer a "join-the-dots" exercise, because if the dots weren't joined by interconnections with the right characteristics, the device would not work!

The designer had a heavy burden of responsibility – the quality of his design could substantially affect the yields of both PCB fabricator and assembler, and efficient design processes were critical to ensure that the product got to market early.

Osmond emphasised the importance of analysing the design early, to save revision spins, eliminate scrap and reduce labour and hardware costs. DfX methodologies ensured an end product fully optimised for the highest overall performance at the most economical unit cost.

He concluded his presentation by connecting a CAD system to the projector and giving a live demonstration of how the engineer interacts with a real design.

Outside of the lecture theatre, during breaks in the proceedings, delegates made the most of the opportunity to visit the tabletop exhibition area and to network with their peers. All round, a very successful and well-balanced event and a credit to the efforts of **ICT Technical Director Bill Wilkie** and the staff of **Tweed Horizons.**

Pete Starkey
ICT Council
June 2008

ICT/IEMRC
Plating Technology Seminar,

Wednesday, 6th August 2008
Loughborough University

Classic English summer - grey skies and rain! But the crowd of eager delegates who gathered at the Wolfson School of Mechanical and Manufacturing Engineering in Loughborough University were there to learn about state of the art metal finishing processes for PCB manufacture, not to escape the weather. The Institute of Circuit Technology joined forces with the Innovative Electronics Manufacturing Research Centre for a Summer Seminar on Plating Technology, introduced by IEMRC Co-ordinator **Dr Darren Cadman** and ICT Technical Director **Bill Wilkie.**

Dave Wayness from **Rohm and Haas** explained in detail how cost and performance of copper electroplating processes could be optimised for different applications, with a sage reminder that technologies could be easily over-sold and that it was important in choosing the right process to understand not only what it did well but also what it did not do well! The days of one-process-fits-all were long past and even different geographical regions now required significantly different functionality to support the design characteristics and end-user requirements of their particular market sectors. He reviewed many permutations: vertical or horizontal processing; DC or pulse rectification; panel, semi-panel or pattern plating; conformal plating or microvia filling; soluble or insoluble anodes, and described how Rohm and Haas had developed a series of copper plating chemistries to achieve specific objectives in high aspect ratio through-plating and via filling, defining "difficulty factors" and "stability indices" to gauge their effectiveness, and using a mathematical model to calculate the cost savings which could be achieved using the appropriate process variant for the job.

Jean Rasmussen from **Cookson** described the technical and environmental benefits of direct metallisation using intrinsically conductive polymers to selectively activate resin and glass without contamination of copper surfaces. Cookson's process worked by first depositing an initiator layer of manganese dioxide, which then acted as an oxidative initiator for the in-situ polymerisation of ethylene-dioxy-thiophene in the presence of an organic sulphonic acid. The conductive polymer was mechanically and thermally stable, and in high-aspect-ratio through-holes, coverage with acid copper was complete and void-free within 60-90 seconds. The process had significant environmental advantages when compared with electroless copper. It contained no formaldehyde or chelating agents, waste treatment was simple and large savings could be made in water consumption, making it particularly attractive to Asian fabricators for whom water was generally a very expensive commodity.

Andy Cobley, sonochemistry specialist from **Coventry University,** reviewed studies of the physical and chemical effects of ultrasound in liquid media, and their potential applications in metal finishing, where traditionally ultrasonics had been used only for cleaning purposes. Explaining the principles of acoustic cavitation, theoretically capable of generating enormously high pressures and temperatures at the point of collapse of microscopic bubbles, and the phenomenon of microjetting, when bubbles collapse asymmetrically at a surface, he demonstrated how increases in limiting current density and current efficiency could be achieved in electroplating as a consequence of disruption of the diffusion layer. In electroless copper plating, the use of ultrasonics simply at the catalyst stage gave a significant increase in the deposition rate of copper, and this increased further if ultrasonic agitation was applied in the copper bath as well. This effect could possibly be exploited in the development of formaldehyde-free electroless copper chemistry.

Martin Bunce from **MacDermid** described recent advances in electroless copper process technology. MacDermid's whole sequence had been designed specifically to maximise the reliability of inner-layer connections, and began with an organo-silane conditioner, which was adsorbed only on to non-conductive surfaces. A tin-palladium catalyst reacted with the conditioned surfaces, whilst depositing very little on copper. The accelerator was unusual in that, instead of dissolving-away the stannous tin, it oxidised stannous to stannic and left it in place as a shield to the palladium nuclei, resulting in slow, controlled initiation of electroless copper. The copper chemistry gave a low-stress deposit with fine grain structure and minimal co-deposition of contaminants. Solder shock and interconnection stress testing demonstrated that, even after the most severe thermal abuse of high layer-count test boards, the interconnections between plated-through-hole and inner layers maintained their integrity.

Brian Reid from **Schloetter** gave a practical account of the development of an acid copper electroplating process to satisfy the demands of smaller UK PCB fabricators who wanted a via-fill process that could be used simultaneously for pattern plating, on standard equipment, with soluble anodes. The result was a high-copper, low-acid formulation with three liquid additives, which combined excellent levelling with good ductility and low internal stress. Typical cycle time was two hours at 1 amp per square decimetre for via filling in pattern plating mode. Although insoluble anodes gave the most consistent results, they were comparatively expensive and soluble copper anodes could be successfully used provided they were removed from the electrolyte during idle periods.

The rain had almost stopped when delegates left the university campus, although it was rumoured that a mature student named Noah was working hard at his CAD system, drawing up plans for an ark....

Pete Starkey
ICT Council

Addressing Environmental Needs

The Institute of Circuit Technology Seminar.
Darlington UK. September 2008

Darlington, in the north-east of England, famous for its association with the world's first passenger rail journey in 1825, was the venue for a well-attended **Institute of Circuit Technology** evening seminar on the theme "Addressing Environmental Needs". The seminar focused upon the impact and mitigation of environmental legislation on printed circuit fabricators and their suppliers. Delegates travelled from all over the UK to attend, accompanied by a deluge of rain that had made its way from somewhere in mid-Atlantic.

Introduced by ICT Technical Director **Bill Wilkie**, **Tom Brown of Holders Marketing**, a Fellow of the Institute, began the evening's proceedings with a paper discussing methods of assessing the potential reliability of laminates during lead-free soldering processes. He explained that simply specifying materials according to IPC 4101 slash sheets might not be sufficient to ensure a particular thermal performance in critical applications. Acknowledging work published by **Werner Engelmair**, Tom explained the derivation of the Soldering Temperature Impact Index, a function of readily available data: glass transition temperature, decomposition temperature and Z-axis thermal expansion coefficient:

STII = Tg/2+Td/2—(TE%(50 to 260°C) x 10)

which gave a meaningful indicator of the thermal stability of a laminate during soldering. An STII-value of 215 or greater was recommended for PCBs of 1.5mm or more in thickness.

Specialist in cleaning processes for electronics assemblies, **Graham Fraser of Fraser Technologies** gave an insight into the types of equipment and chemistries currently available, and reviewed both solvent and aqueous systems. He explained that there was no single ideal system, and many factors needed to be taken into account such as current and local legislation directives, level of cleanliness required, volume of circuits to be processed, component and bare board compatibility, as well as available space with respect to equipment footprint. Cost was clearly an important issue. At the lower-cost end of the scale were small batch-type processes in both solvent and aqueous chemistries. Then came the sealed solvent and larger in-line aqueous systems capable of high volume throughput, all of which had to meet and exceed current environmental directives. Graham emphasized that systems should be chosen on the basis of total cost of ownership, rather than on consumable costs, and that increasing power and water costs were significant factors regardless of which system was adopted. He described a "Cost of Ownership Model" designed to provide information to enable customers to make informed purchasing decisions.

Always a popular speaker at ICT events, **Enthone's Frando van der Pas** debated the question **"Do Green, Performance and Cost go together in PCB manufacturing?"** Against a background of relentless environmental legislation and fierce competition, PCB fabricators were striving to reduce costs throughout the whole of the manufacturing process whilst continuing to maintain demanding standards of product quality and performance. Suppliers of chemical processes recognised these challenges and had responded by developing chemistries which were less waste generating, required less rinse water and operated at lower temperatures. Examples were oxide-replacement inner layer bonding treatments with low etch factors and high copper capacity, direct metallisation processes based on conductive polymer technology as technically and environmentally superior alternatives to electroless copper, and lead-free solderable finishes – immersion silvers and OSPs – as alternatives to HASL and ENIG. All of these processes were enabling technologies which offered reduced costs whilst providing significant environmental benefits.

Paul Watson of CEMCO – FSL, another Fellow of the Institute, presented the final paper which focused on **saving energy and reducing waste from the equipment supplier's perspective.** In the past, few manufacturers of wet process equipment had been particularly conscious of the need to produce systems that were waste and energy efficient. Equipment development had been driven by panel technology and size, requiring wider machines with transport systems that could convey thinner and thicker product with finer lines, smaller holes and irregular shapes etc. As a consequence, equipment had become more complicated with high operating costs in terms of power consumption and waste produced. Paul reviewed in detail the criteria driving current equipment development: lower volume sumps, improved liquid flow dynamics of chemistry and rinse water, improved fluid containment, more efficient drying systems, integration of controlled water/chemical usage and waste management, and reduced footprint size, and described some of the innovative features of new-generation wet-processing machinery.

In his closing remarks, **Bill Wilkie** commented that this had been the second successful ICT Evening Seminar to be held at the Devonport Hotel in Darlington this year, both events having been exceptionally well attended. He gratefully acknowledged the support of :-

Gordon Arkley
of Faraday Circuits
who had sponsored the event.

Pete Starkey
ICT Council
September 2008

Printed Circuit Board Quality & Failure Analysis Workshops
– Special discount for all ICT Members

Three new workshops combining both theoretical and hands on sessions allow engineers and PCB & Assembly buyers to see how to assess and maintain incoming printed board quality are being run by ITRI and Bob Willis. These sessions are being held at the laboratories of ITRI Innovation in St Albans, Hertfordshire. The workshops will be led by Bob Willis and assisted during the laboratory based practical session by the ITRI Laboratory Manager Dr. Wayne Lam.

PCB Inspection & Quality Assessment – Practical Solutions Workshop Tuesday 24th March
Troubleshooting Your Assembly Yields - On Site or Offshore Workshop Wednesday 25th March
Step by Step Electronics Failure Analysis Workshop Wednesday 22nd April

For further information go to www.ASKbobwillis.com/PCBworkshopict.pdf

By sourcing PCBs from overseas or through distributors it can sometimes be difficult to assess the quality of incoming substrates. The switch to using lead-free assembly processes has highlighted issues of poor quality design and poorly fabricated circuits; thereby the need to understand available test methods is ever more important. Assembly yields and failure analysis techniques are also covered in these new workshops and are an ideal balance of theory and practical knowledge. By holding these events at the ITRI Laboratory delegates can witness the various techniques available for the verification of acceptable quality using a range of specialised techniques which are not always available in their own facilities.

"As the supply chain grows longer the ability to monitor and maintain the quality of incoming PCBs becomes crucial. We believe that this new workshop will offer those designing and specifying circuit boards a chance to assess and measure the quality of incoming products in a cost effective manner. This workshop comes in response to a growth in PCB laminate issues we see coming into our laboratories in the last year or two. Working in conjunction with Bob Willis we can offer PCB inspection, testing, on-site process audits, and now training workshops" says Tom Perrett, the ITRI Marketing Manager.

The workshops would benefit PCB designers, process and quality engineers responsible for specifying and inspecting printed boards. The cost of the workshop session is £175 + VAT and includes refreshments, workshop notes and a set of colour wall charts featuring the most common PCB defects. All ICT members will receive a discount of £25. The workshop will take place from 9.30am to 4.30pm.

To book your place go to www.ASKbobwillis.com/PCBworkshopict.pdf

The Membership Secretary's notes September 2008

It isn't often that we get the opportunity to present new certificates to Members in person, but I called in at Faraday Circuits on my way down to the Darlington Seminar, this September and was able to present Les Blakeman with his upgrade to be a Member Institute of Circuit Techmology.

This was our second Seminar to be held at the Devonport Hotel, on the river Tees at Darlington and the high turnouts have guaranteed that it won't be the last!

We have also been busy with other events since the last journal, with a Southern Symposium on the Effect of Environmental Legislation down at Waterlooville and a new event at Loughbourough University. We held this event, an afternoon Symposium, in conjunction with the IeMRC group at the University, on Plating Technology and again, the high turnout means that we will try and repeat this joint event next year.

Our events not only provide an opportunity for Members and guests to meet and network, but also for non-members to see what we are like and hopefully apply to join the Institute. We welcome both Richard Houghton, who joined at our Loughborough event and Eric Hinsley, who joined at Darlington.

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