Journal of the

Institute of Circuit Technology

Vol.11 No.1 Winter 2018

2017 Events

19th September **ICT Evening Seminar**
at Newtown House Hotel,
Hayling Island
bill.wilkie@InstCT.org

5th December **ICT Evening Seminar**
at Majestic Hotel, Harrogate
bill.wilkie@InstCT.org

2018 Events

13th March *Tuesday* **ICT Evening Seminar & AGM**
at the Besf Western plus Manor Hotel, Meriden
bill.wilkie@InstCT.org

9th-12th April **Annual Foundation Course**
at Chester University.
bill.wilkie@InstCT.org

5th June **Annual Symposium**
at the Beaulieu Motor Museum
bill.wilkie@InstCT.org

Editorial

Dear Members

Please accept my apologies for the delay in publishing this issue of the *Journal* . It was entirely my fault that I couldn't make the "e-mail" work, and other foolish mistakes.

Bruce Routledge - Editor

Membership *New members notified by the Membership Secretary*

Membership No.	Name	Company	ICT Grading	Notation
10429	Mike Wright	DK Thermal	Member	M.Inst.C.T.
10430	Gavin Kettlewell	DK Thermal	Member	M.Inst.C.T.
10431	Tim Tatton	Amphenol-Invotec	Fellow	F.Inst.C.T.

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9957	David Pike F.Inst.C.T.	Graphic Electronics
10151	David Maitland F.Inst.C.T.	CCE
10202	Emma Hudson F.Inst.C.T.	UL UK
10267	Steve Lloyd F.Inst.C.T.	GSPK

2017 MEMBERSHIP REVIEW

Grade	Base	31 Dec 2010	31Dec 2011	12Jul 2012	31Dec 2012	31Dec 2013	31Dec 2014	31Dec 2015	31Dec 2016	31Dec 2017
Associate	24	64	64	91	90	94	114	131	151	170
Member	45	108	119	122	133	142	128	140	143	143
Fellow	26	65	69	66	68	66	72	73	70	77
Hon.Fellow	4	10	10	10	11	11	13	11	10	10

It is the policy of the Journal to correct errors in the next issue

Please send corrections to : -

brucer @ john lewis.com

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Solder Limits: Updating Them for the Age of Surface Mount

by **Emma Hudson, UL PCB Industry Lead for EMEA+LA region**

Lead PCB Engineer for Europe and Latin America with UL

Emma Hudson

What are Solder Limits?

Solder Limits are one of the fundamental parameters we use when evaluating the PCB, solder resists, and metal clad base materials for safety under the UL Recognition programme.

Solder Limits are designed to represent the soldering processes the PCB will be exposed to during the component assembly operations. They consider any time that is spent over 100°C or the Maximum Operating Temperature (MOT) of the PCB, whichever is greater. The only exception to this is that hand soldering operations do not need to be captured in this assessment.

They can be a single time and temperature, such as 288°C for 20 seconds, or multiple solder limits (MSL) that include multiple times and temperatures and can also include ambient periods to represent time between different soldering operations.

The solder limits are used as part of the thermal shock procedure employed prior to many of the tests employed to evaluate the PCB for safety.

How to Interpret the Solder Limits

As previously mentioned, the solder limits consider any time spent over 100°C or the Maximum Operating Temperature (MOT) of the PCB, whichever is greater. To determine if the Recognized Solder Limits are being exceeded we need to understand the soldering operations the PCB will be exposed to and the thermal profiles associated with these. We then use these thermal profiles to measure the time above the critical temperature.

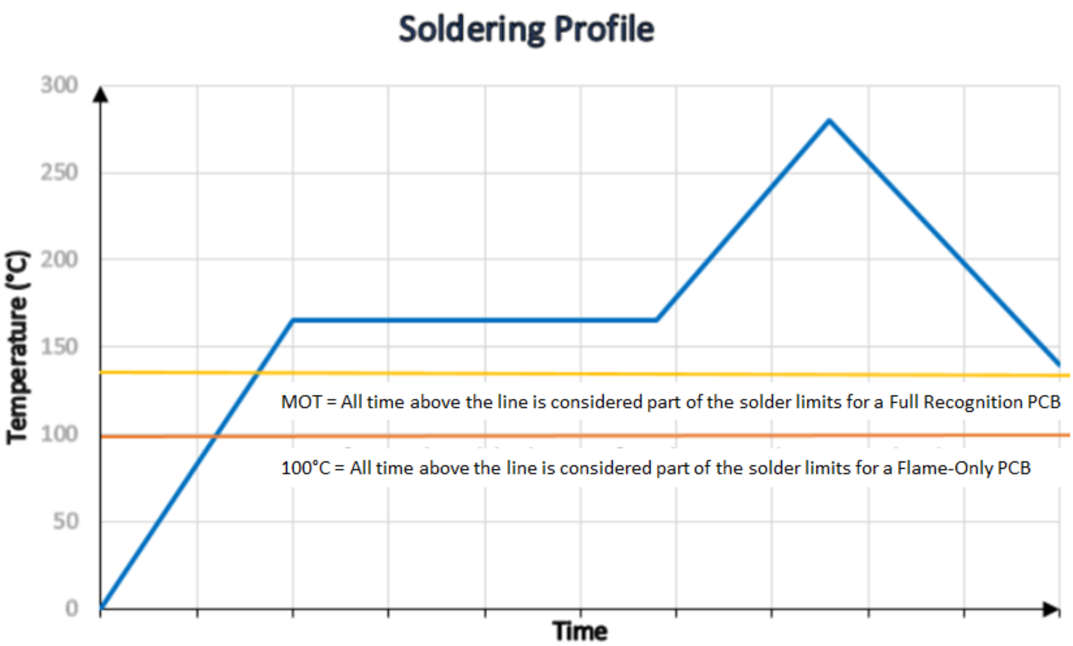


Figure 1: Generic SMT Profile showing how to measure the time for the Solder Limits parameter

Figure 1 shows a generic Surface Mount (SMT) type soldering profile; we can use this to determine the time spent over either 100°C or the MOT Recognized for the PCB. If the board has a Flame-OnlyRecognition then we determine any time spent over the 100°C line. For a Full Recognition PCB it is any time spent over the MOT line.

When you look at the total time above the line you can see why using multiple solder limits with different times at different temperatures becomes more appropriate for soldering profiles of this type, otherwise you would be looking at a long period of time at a high temperature.

The way we deem compliance with the solder limits can be seen in Figure 2, this provides an example for a Flame-Only Recognized PCB with solder limits of 288°C for 20seconds. If the t_1 to t_2 period is greater than 20 seconds then the solder limits have been exceeded and the UL Recognition of the PCB has been invalidated. In Figure 3 we can see the same evaluation being made but for a PCB Recognized with an MOT of 130ºC.

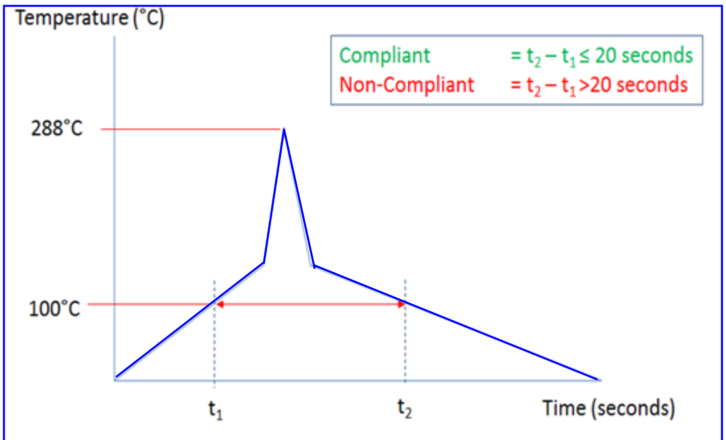


Figure 2: Determining compliance of a Flame-Only PCB Recognized with Solder Limits of 288°C for 20seconds

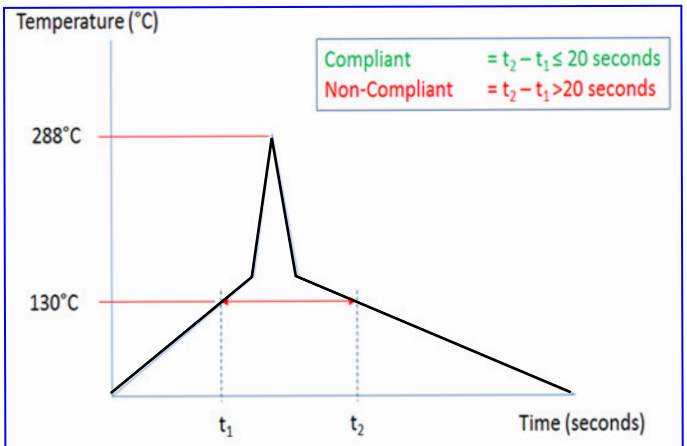


Figure 3: Determining compliance of a Full Recognition PCB with a 130°C MOT and with Solder Limits of 288°C for 20seconds

If a PCB is Recognized with Multiple SolderLimits (MSL), an example shown in figure 4, then the PCB can be exposed to temperatures between 100°C and the temperatures detailed for the time shown, these are in addition to each other and not alternatives to one another.

EMC-T

Multilayer printed wiring board made from prefabricated type (mass laminated) industrial laminates FLAMMABILITY ONLY Recognitions

Cond Width Min (mm)	Cond Width Edge (mm)	Cond Thk Min (mic)	Cond Thk Max Int (mic)	Cond Thk Max Ext (mic)	SS/ DS/ DSO	Max Area Diam (mm)	Solder Limits Temp (C)	Solder Limits Time (sec)	Max Oper Temp (C)	Flame Class	Meets UL796 DSR	CTI
-	-	-	-	-	DS	-	180	10800	-	V-0	-	-
							230	80				
							260	10				
							23	300				
							260	10				

Figure 4: Example of a Flame-Only Recognized PCB with Multiple Solder Limits

For the example shown, this means 10800 seconds between >100°C and 180°C plus 80 seconds between >100°C and 230°C plus 10 seconds between >100°C and 260°C plus minimum of 300 seconds at ambient plus 10 seconds between >100°C and 260°C.

Why are the Solder Limits So Important?

The IPC D-32 Thermal Stress task group have conducted research that has shown that PCBs that pass a solder float test can fail during surface mount assembly soldering operations, which is not surprising to those of us in the PCB industry. We have been aware for a long time that the more severe the soldering operations are the greater the degradation of the PCB. The increased degradation impacts not just the reliability properties of the PCB but also the properties we evaluate for safety.

For UL to conduct an accurate safety assessment of the PCB we MUST use Solder Limits that are representative for the actual soldering processes the PCB will see during assembly operations; if we use inadequate Solder Limits during the testing than are intended for use in production then it invalidates the safety testing that has been conducted on that PCB, as we cannot be confident that the PCB will behave the same after being exposed to these more severe conditions.

What UL is Doing to Help the Industry

One of the main things we get told at UL when it comes to the PCB manufacturer selecting the solder limits they want to use for Recognizing their PCB in combination with is that they do not know what soldering profiles their customers will use. Coming to UL from a tier-1 automotive electronics manufacturer I completely appreciate this point, I never told my PCB suppliers what soldering profiles I was using on my boards and I was just one of many customers to that PCB company. So what we, UL, are doing is to offer some standardised soldering profiles for the PCB manufacturers to use for Recognition purposes.

We are taking the IPC-TM-650 2.6.27 T230 and T260 soldering profiles and offering these as an option for the PCB manufacturers to use. These are will only ever be optional and we will not force anyone to go down a specific route. We are also happy to use any other reflow profile a PCB manufacturer requests to be used.

UL is recommending a minimum of three reflow cycles but the PCB manufacturer needs to understand the maximum number of cycles their customers may need. Recent suggestions of six cycles have been made by one contract assembler!

We are endeavouring to add these IPC T230 and T260 soldering profiles to UL 796 – the standard used to assess PCBs – but this is not a requirement for them to be used by manufacturers, it would only be as a more accessible guideline / option. UL do not control what goes into the UL standards, this is done through a consensus process where UL has only a single vote on the Standards Technical Panel (STP); we have been trying to add these profiles to the standard for some time but hope that the STP will see the value in us doing this now and they will enter the standard shortly.

UL are very open to having other standardised reflow profiles added to the standard and are happy to receive suggestions on this.

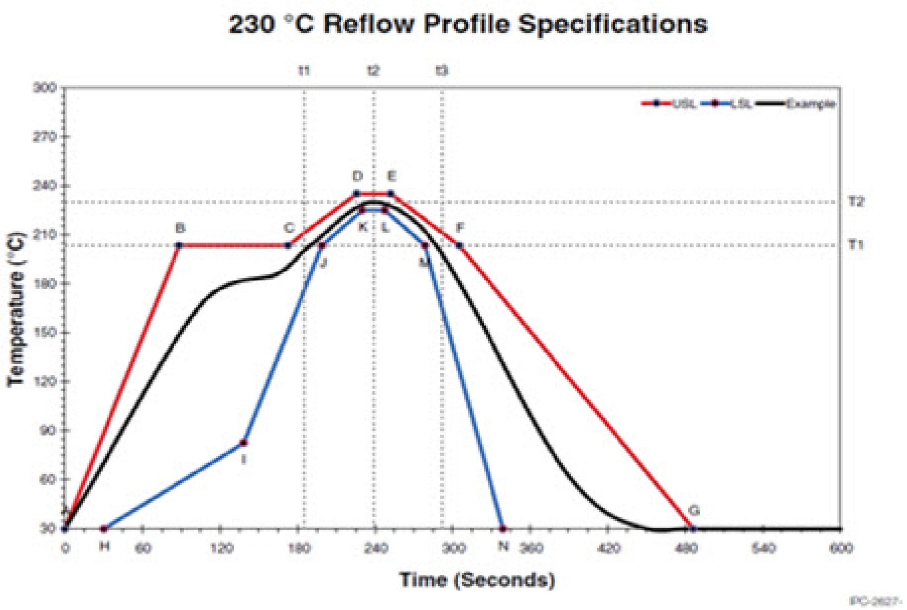


Figure 5: IPC TM-650 2.6.27 T230 soldering profile

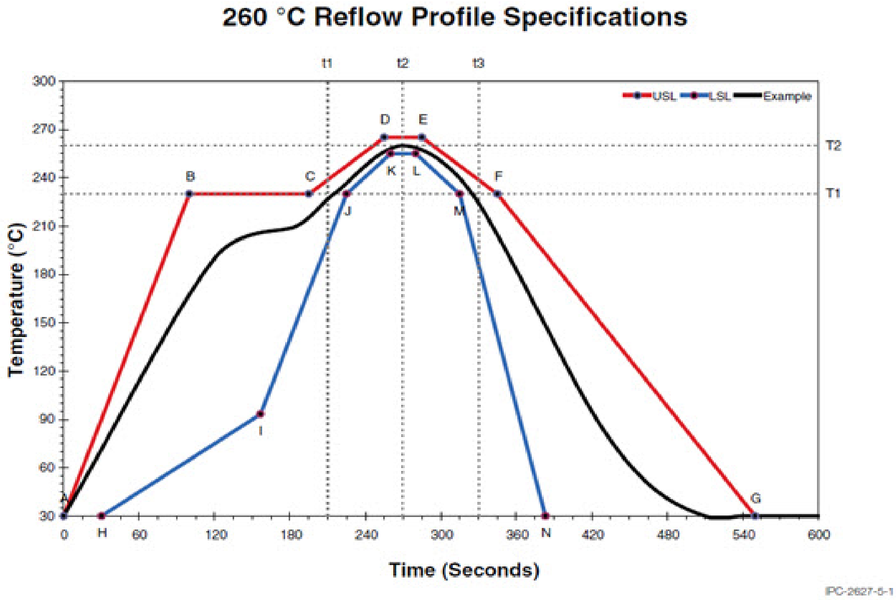


Figure 6: IPC TM-650 2.6.27 T260 soldering profile

It is not intended that UL will create its own reflow profiles.

<table>
<tr><th rowspan="3"></th><th colspan="5">Example Rigid Multilayer Construction</th></tr>
<tr><th colspan="2">First Base Material</th><th colspan="3">Subsequent Base Materials</th></tr>
<tr><th>Full Recognition PCB</th><th>Flame-Only PCB</th><th colspan="2">Full Recognition PCB</th><th>Flame-Only PCB</th></tr>
<tr><td rowspan="2">Bond Strength & Delamination</td><td rowspan="2">Yes</td><td rowspan="2">N/A</td><td colspan="2">Check to see if CCIL Program requirements are met</td><td rowspan="2">N/A</td></tr>
<tr><td>CCIL Met = DOMSA on each material</td><td>CCIL Not Met = BDMSA on each material</td></tr>
<tr><td rowspan="2">Flammability</td><td rowspan="2">Yes</td><td rowspan="2">Yes</td><td colspan="2">Check to see if CCIL Program requirements are met</td><td rowspan="2">V test each material</td></tr>
<tr><td>CCIL Met = no additional V testing</td><td>CCIL Not Met = V testing on each material</td></tr>
</table>

BDMSA - 10/56-day Bond strength and delamination testing with micro-section analysis

DOMSA - 10/56-day Delamination testing with micro-section analysis

V - UL 94 Vertical Flammability testing

Figure 7: Assessing the Testing Needed to Increase Solder Limits for a Recognized PCB – Metal Clad Base Materials

	Example Rigid Multilayer Construction		
	First Solder Resist	Subsequent Solder Resists	
Flammability	Yes	Check to see if Permanent Coating Program requirements are met	
		Permanent Coating Program Met = no additional V testing	Permanent Coating Program Not Met = V testing on each material

V - UL 94 Vertical Flammability testing

Figure 8: Assessing the Testing Needed to Increase Solder Limits for a Recognized PCB – Solder Resists

Each UL/ANSI grade of base material would need to be assessed, so if a board has both FR-4.0 and FR-4.1 materials detailed for use the complete testing would need to be done on each UL/ANSI grade before we could look to apply the CCIL/MCIL Program.

One problem that PCB manufacturers are likely to face is that the vast majority of base materials and solder resists have not been Recognized in combination with solder limits suitable for SMT reflow profiles, which in turn means that the CCIL / MCIL Program cannot be used for the base materials and the Permanent Coating Program for the solder resists, as the solder limits of the material have to be equal or more severe than the PCB it is being added to for these reduced test / no-test programmes to be considered. If the solder limits of the materials are not suitable, each base material would need to be evaluated for Bond Strength, Delamination, and Flammability and each solder resist for Flammability.

UL will endeavour to communicate the meaning of the solder limits to all relevant parties but the PCB manufacturers need to help us and work with their suppliers to insure they are using the appropriate solder limits when Recognizing their materials such that the CCIL Program and Permanent Coating Program can be routinely used to minimise the testing required for the PCB manufacturer.

We strongly recommend any new PCB be Recognized with solder limits suitable for SMT reflow soldering, unless the PCB manufacturer is 100% confident that the PCB will never be exposed to soldering of this type.

What is Going to Happen Moving Forward?

UL intends to actively communicate this message to the relevant parties – OEMs with UL Listed products, Recognized PCB assemblers and PCB manufacturers, and Recognized material manufacturers supplying the PCB industry. The intent is to send out a Bulletin to all of these parties to ensure everyone understands what solder limits are and that anyone who has a requirement to use a Recognized PCB MUST ensure that the solder limits of the PCB are not exceeded during the soldering processes for the Recognition to still be considered valid.

UL are also attempting to have the PCB standard – UL 796 – updated with the standardised IPC TM-650 2.6.27 T230 and T260 soldering profiles, as mentioned previously. It is not a requirement to have these thermal profiles in the standard for the PCB manufacturer to request to use these but we feel it will make it easier for the industry to request them if they are presented as an option.

From the start of 2018 ULs Follow-Up Service (FUS) inspectors will receive refresher training about what solder limits are and how to interpret them when inspecting the PCB assemblers and OEM. The inspectors will be asking to see evidence of the soldering profiles any Recognized PCBs have been exposed to during any assembly operations and they will check that these have not exceeded the

Any time a Recognized PCB is found to have exceeded the Recognized solder limits for that board it will be deemed to not be in compliance and a Variation Notice will be raised and further action will be needed to resolve the matter.

Ideally the assembler and/or OEM will let the PCB manufacturer know what solder limits they need their UL Recognized PCB to have but we know this happens very infrequently, so it is important for the PCB manufacturer to take the initiative and start Recognizing their PCBs in combination with soldering profiles suitable for the world of multiple surface mount soldering operations.

Summary

The Solder Limits for the vast majority of Recognized PCBs are not representative of the Surface Mount soldering operations that are common place within the assembly industry today and this has to be fixed. The PCB industry has been well aware for many years that the more severe the soldering processes the greater the degradation of the PCB; typically we consider the degradation with regard to the reliability of the PCB but it is just as valid when considering the safety elements. For the safety assessment to be valid, the PCBs must have been evaluated in combination with Solder Limits that represent the actual soldering processes the board will be exposed to in production. The traditional solder float test is not valid for a PCB that will be exposed to SMT soldering operations.

UL want to make it easier for the industry to be able to assess their PCBs and their materials in combination with soldering profiles for the SMT age and are offering the IPC TM-650 2.6.27 T230 and T260 as an option for the safety evaluation. The industry can select any other profile they wish but we often hear that the PCB manufacturer does not know the reflow the profile that will be needed, so we hope by offering some industry standard profiles this will help all parties in doing the right thing.

Testing is going to be needed to bring PCBs already Recognized with single time / temperature solder limits up to these SMT soldering profiles but this could be minimised if laminate and solder resist manufacturers can be convinced to also bring their Recognized solder limits up to meet these. We would certainly recommend all new PCB types being evaluated use SMT style solder limits. The industry must address this; the solder limits have to represent the soldering processes the PCB will be exposed to.

The final message I would like to leave you with is that we are here to help you with this! Any questions or concerns, any help needed, please contact me and I will do what I can to assist you through this process and make sure your PCBs are ready to be used for the SMT soldering profiles that are so commonplace in our industry today.

Emma Hudson,

UL PCB Industry Lead for EMEA+LA region

Review of :-

Institute of Circuit Technology Harrogate Seminar 2017

by **Pete Starkey**

Bill Wilkie

Emma Hudson

A return to the historic spa town of Harrogate in Yorkshire, England for the Institute of Circuit Technology Northern Seminar, to enjoy a diverse programme of presentations on safety standards, research in selective metal deposition, and developments in imaging and inspection techniques.

After extending a warm welcome to delegates and acknowledging the support of sponsors Fineline VAR, ICT technical director **Bill Wilkie** began by reminding members of the value of the Institute website as a source of essential information. He made particular reference to the BSI page and recent controversy about proposals by IEC TC111, where as a result of the Institute's representation on BSI standards committees, members had early warning of a potential ban on PTFE laminates, which put them in a strong position to lobby against it.

He introduced as first speaker the ever-popular **Emma Hudson**, Lead PCB Engineer for Europe and Latin America with UL, who has made it her vocation to help the PCB industry through the safety certification process. Her topic was Solder Limits, and bringing them up-to-date in respect of surface-mount assembly processes. The thermal stresses experienced in surface mount assembly could be considerably more severe than those typically represented by a traditional solder-float test. Therefore for an accurate safety assessment of the PCB, it was essential that Solder Limits meaningfully represented the actual soldering processes the PCB would be exposed to during assembly operations. If the Recognized Solder Limits were exceeded in production then the Recognition, in effect the safety assessment, would be invalidated, because the more severe the soldering operation, the greater the degradation in the properties of the PCB evaluated for safety. Hudson made it clear that UL acknowledged the existence of many different product-specific soldering profiles, and the difficulties faced by PCB manufacturers in choosing which profiles to use for Recognition to meet all their customers' needs. In an effort to help the industry, UL would be offering standardised soldering profiles for Solder Limits to make their implementation easier. These were based on IPC-TM-650 2.6.27 T230 and T260 reflow profiles as a default option to represent tin-lead and lead-free SMT soldering, although bespoke profiles and additional wave-solder-type soldering limits could be requested. And UL were also attempting to add a reference to these profiles into UL 796 for guidance.

She described the procedures for updating Solder Limits for different base materials and multilayer constructions, explaining where the CCIL Program could and could not be used, and went on to discuss procedures for solder resist, with examples of when the Permanent Coating Program could and could not be used. And she urged PCB manufacturers to push their suppliers to Recognize their materials with suitable Solder Limits. Furthermore, she strongly recommended Recognizing any new PCB with the new solder limits, whether materials were Recognized with these requirements or not, and to contact UL for assistance sooner rather than later. "Do it before your customer contacts you!"

UL aimed to actively inform all relevant parties: PCB manufacturers, material manufacturers, Recognized PCB assemblers and OEMs with UL Listed products. UL follow-up services would commence in 2018, and UL would require to see evidence of the actual soldering profiles used for the PCB assembly, to confirm that the soldering processes to which the PCB had been exposed did not exceed the Recognized solder limits and so invalidate the Recognition.

ICT Chairman Andy Cobley

The second presentation came from **ICT Chairman Andy Cobley**, recently appointed Professor of Electrochemical Deposition at Coventry University, who gave an insight into current research on magnetic-field-enabled selective metallisation of dielectric substrates. Previous research on the effects of a magnetic field on electrochemical deposition had demonstrated that placing a magnetised iron template behind a conductive substrate induced a magnetohydrodynamic effect which caused changes in the distribution, morphology and crystal structure of electroplated metals, and offered scope for selective deposition. The current work studied magnetic and magnetohydrodynamic effects in the electroless deposition of metals on non-conductive substrates as a potential means of creating conductive patterns. Cross-sections of electroless nickel-boron deposited with and without an applied magnetic field showed significant differences in grain structure, and the magnetic field gave an increase in deposition rate. Classical electroless deposition on a non-conductive surface required a catalyst such as colloidal palladium to initiate the reaction, but this had no magnetic properties. Therefore a material was sought which had both catalytic and magnetic properties, and it was attempted to design and synthesise magnetic/catalytic nanoparticles that could be selectively deposited on a non-conductive substrate using a magnetic field, and to demonstrate that these would initiate electroless copper deposition. The concept was to produce particles with a magnetic core and a catalytic shell, based on Fe_3O_4 iron oxide and silver, by a two-stage process starting with ferrous sulphate and silver nitrate and using arginine as reducing agent. In the event, the resulting nanoparticles were shown to be a composite, with the silver predominantly in the core. However, they proved to have catalytic properties, and to successfully initiate electroless copper deposition. Their efficiency varied depending on concentration, dispersing agent and pH.
Initial trials had shown that the particles could be selectively deposited on a thin FR4 substrate by placing a magnetic template behind it, and electroless copper could subsequently be deposited on the catalysed area. Proposed future work included further study of the magnetic properties of silver-iron oxide nanoparticles, the synthesis of copper-iron oxide nanoparticles as an alternative to silver, and the removal of iron by dissolution after selective catalysation and before electroless deposition, as well as a comprehensive investigation of the effects of process parameters. Coventry University's IP had been secured by patent, and the team was keen to find commercial partners and to identify possible applications of the technology.

Jean-Paul Birraux

In the third presentation, **Jean-Paul Birraux**, sales and marketing manager with First EIE in Switzerland, discussed developments in photo-plotters, UV direct imaging and automatic visual inspection systems. He commented that when he first joined the company in 1999, its former president had predicted that the market for photoplotters would continue only for five years before direct imaging technology would make silver halide films obsolete. In fact the present-day photoplotter market remained strong and there was a demand for higher resolution, higher speed and larger format machines, driven by the manufactures of shadow masks and OLED screens, for example 2.4m x 1.6m with +/- 10 micron accuracy. There was increasing use of long flexible circuits as replacements for wiring harnesses in automotive and avionics applications, and in development was a plotter with unlimited length capability for applications in this sector.

Meanwhile there had been ongoing development in direct imaging technology, and again the trend was to larger-format machines for panel sizes up to 6m x 1m. Light sources with a continuous spectrum from 360nm to 450nm gave a good combination of surface cure and through cure on solder masks. Advances in digital-micro-mirror-device (DMD) technology, using a collimated UV arc-lamp source and a single DMD head, offered a cost-effective and low-maintenance option, enabling very high exposure energy, up to 1000 mJ/cm2 with 20 micron line and space capability.

And in the field of machine vision systems, a new generation of automatic visual inspection equipment had been developed, with the capability to create a master reference image from a single sample, and to inspect both sides of a 240mm x 240mm circuit in a third of the time taken by a human inspector, capturing defects to the 20 micron level. There was also an increasing demand for continuous roll-to-roll inspection.

Andy Cobley & Mike Wright

Andy Cobley brought proceedings to a close and presented Mike Wright, Global Quality Representative for DK Thermal, with his Membership certificate.

As ever, the ICT Northern Seminar provided a platform for the dissemination of knowledge, the sharing of experience and the broadening of a network of PCB professionals. And thanks again to Bill Wilkie for his hard work in organising and coordinating an excellent event.

Pete Starkey

I-Connect007
December 2017

Magnetic Field Enabled Selective Metallisation of Dielectric Substrates

by S.Danilova, J.E. Graves, A.J Cobley

Professor of Electrochemical Deposition at Coventry University

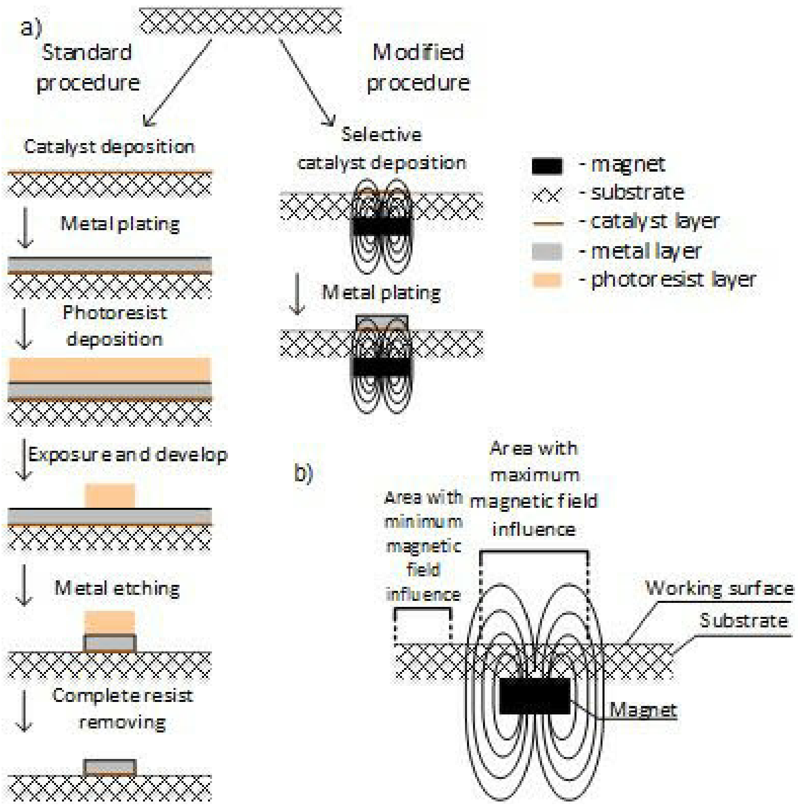
ICT Chairman Andy Cobley

Abstract

The present research suggests a simple and cheap alternative to the existing approaches to selective metallisation of dielectric substrates. It requires minimum equipment and reduces the amount of toxic chemicals involved. This novel approach is enabled by the development of a new type of catalyst which not only initiates electroless deposition but which can also be manipulated using a magnetic field. This new catalyst is a Fe_3O_4-Ag nanocomposite which can be selectively deposited from solution onto the substrate surface by application of a gradient magnetic field. Subsequent electroless copper plating was catalysed by the deposited particles, so that copper is selectively coated in the pattern of the deposited nanocomposite catalyst. In this way, the concept of selective metallisation of dielectric substrates facilitated by magnetic field application has been proven.

Introduction

The selective metallisation of dielectric materials is commonly used in electronic manufacturing. It is usually achieved by photolithography (Figure 1(a)) although a number of alternatives are being investigated in order to simplify the process, reduce the cost and decrease usage of toxic chemicals [1-3].



Figures 1. (a) – the schematic comparison of standard selective metallisation process (left) and the modified method (right), (b) – the set-up of magnet attachment.

There are a number of works showing that patterned metal deposition can be achieved by application of the gradient magnetic field during electrodeposition of metals [4-6]. The gradient magnetic field induces micro-magnetohydrodynamic effects which cause electrodeposits to grow thicker in the area of maximum magnetic field influence leading to patterned metal deposition. However, such 'selective metallisation' can only be achieved on conductive substrates.

The current research was aimed at achieving selective metallisation of dielectric substrates by the application of a gradient magnetic field during the electroless plating process. It was proposed to synthesise new magnetic-catalytic nanoparticles i.e. nanoparticles that would be catalytic to the initiation of electroless copper plating but that were also paramagnetic and could therefore be selectively deposited on a dielectric substrate by means of a gradient magnetic field. Subsequent electroless deposition of metal would therefore occur exclusively where the catalytic-magnetic material had been deposited enabling selective metal deposition (Figure 1(b)).

Methodology.

The new magnetic-catalytic nanoparticles were synthesised using a procedure based on previous work [7]. Iron oxide nanoparticles were first produced and then mixed with silver nitrate using arginine as a reducing agent. The synthesised nanoparticles were collected, washed and dried before being dispersed in Reverse Osmosis (OR) water and the pH of the solution adjusted. The synthesised particles were characterised using Scanning Electron Microscopy (SEM) energy dispersive X-ray spectroscopy (EDX) and Dynamic Light Scattering (DLS) particle size analysis.

The dielectric material was a FR-4 plastic substrate cut into 30x30x2 mm pieces. A Ni-Cu-Ni plated NdFeB magnet with dimensions of 10x5x2 mm was attached to the rear of the substrate.

The electroless copper process was supplied by AGAS Electronic Materials Ltd and consisted of Circuposit Conditioner 3320A and Electroless Copper 3350. However, the standard Pd-Sn catalyst was replaced with the new magnetic-catalytic nanoparticle catalyst produced as described above. The following procedure was therefore used;

1. *Circuposit Conditioner 3320A 50ºC 5 min*
2. *Magnetic-Catalyst 20ºC 30 sec*
3. *Electroless Copper 3350 46ºC 25 min*

Images of the deposited copper and catalyst film were obtained using an optical microscope.

Results.

The SEM EDX analysis (Figure 2 (a) and (c)) confirmed that in the first stage of the synthesis Fe_3O_4 nanoparticles had been synthesised with an average size distribution of 369 nm (Figure 2 (e)). The images of the nano-material produced after stage 2 of the synthesis revealed larger nanoparticles of size 8319 nm (Figure 2 (e)) and SEM-EDX analysis confirmed the presence of both (Figure 2 (b) and (d)). This analysis suggested that a nanocomposite Fe_3O_4 and Ag material had been synthesised.

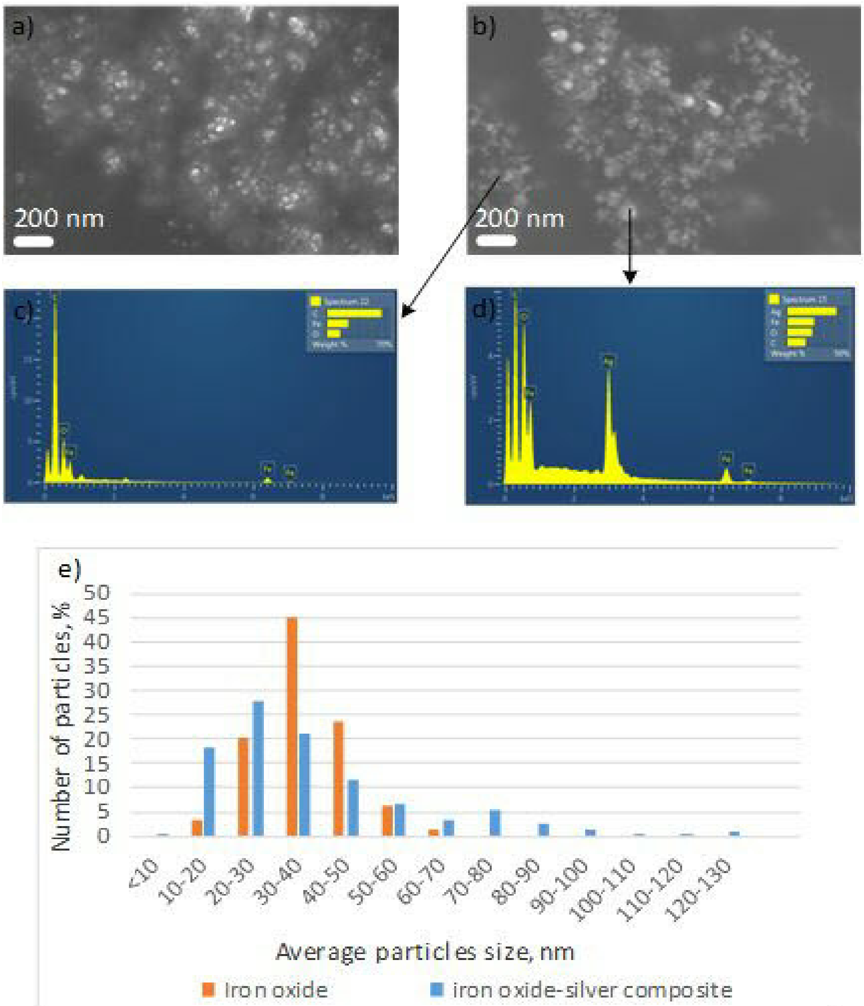


Figure 2. The SEM images of synthesised (a) - Fe_3O_4, (b) – Fe_3O_4-Ag, (c, d) - the results of EDX analysis, (e) – the comparison of the Fe_3O_4 and composite Fe_3O_4-Ag nanoparticles size distribution

The obtained material was dispersed in RO water at various pH values. Figure 3 shows that subsequent selective metallisation of electroless copper was strongly dependent on the pH of the catalyst solution with the most consistent deposit being obtained at pH 2.

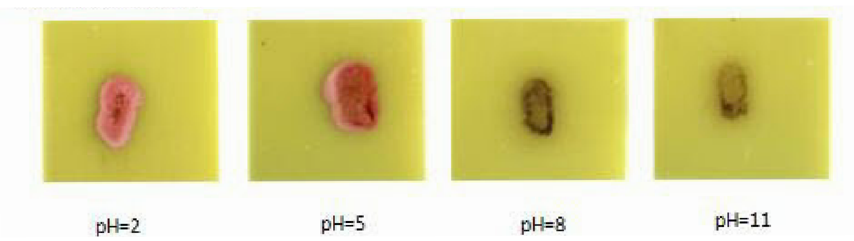


Figure 3. The images of selectively metallised surfaces activated by catalyst solution with a different pH level.

At higher pH, although the catalytic-magnetic material still demonstrated magnetic properties and was selectively deposited on a dielectric material at the area of maximum magnetic field, the catalytic properties of the material were poor. This suggests that there is no composite formation of Fe_3O_4-Ag particles in the solution. This could be attributed to a change in the electrostatic interaction between nanoparticles. The surface charge of Fe_3O_4 and Ag nanoparticles changes at different pH levels [8, 9] and the attraction between nanoparticles is present only when the surface charges have opposite values. According to previous studies, attraction between particles could be achieved at an acidic pH, where Ag has a negative charge and the Fe_3O_4 is positive. At neutral pH, Fe_3O_4 particles become isovalent and the attraction almost disappears. At basic pH the Fe_3O_4 and Ag both have a negative surface charge which can cause particle repulsion and decomposition of material.

Figure 4. (a) The optical image of the selectively deposited composite Fe_3O_4 – Ag catalyst (b) the optical image of the selectively deposited copper layer.

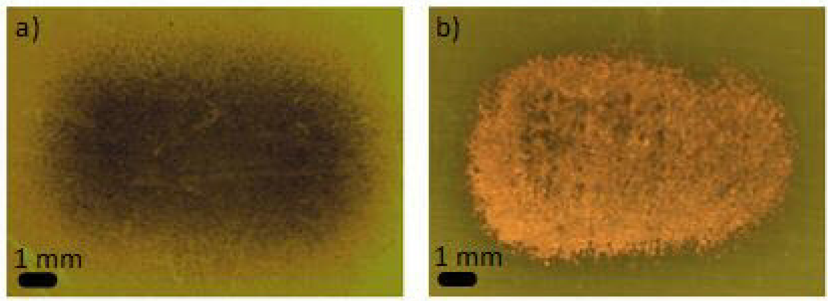


Figure 4.(a) The optical image of the selectively deposited composite Fe_3O_4 – Ag catalyst (b) the optical image of the selectively deposited copper layer.

Figure 4 (a) shows the appearance of the FR4 substrate after immersion in the acidic magnetic-catalytic nanoparticle solution and clearly shows that the catalyst has only been deposited in the area of the maximum magnetic field. In Figure 4 (b) it can be seen that subsequent electroless copper plating occurred exclusively where the magnetic-catalytic nanoparticles had been deposited. The concept of selective metallisation of dielectric substrates using a gradient magnetic field and magnetic-catalytic nanoparticles had therefore been proven.

Conclusion

A dielectric substrate was selectively metallised by using a gradient magnetic field and a modified catalyst. The synthesised composite Fe_3O_4-Ag material shows magnetic properties and catalytic activity for use in the copper electroless plating process. The optimal pH for the implementation of a new type of catalyst was found. The present research proved that selective metallisation can be achieved by gradient magnetic field application.

Reference list

[1] H. J. Gysling, Nanoinks in inkjet metallization — Evolution of simple additive-type metal patterning, J. Colloid. Interface Sci., 19 (2014) 155–162.
[2] H. Asoh, S. Sakamoto, S. Ono, Metal patterning on silicon surface by site-selective electroless deposition through colloidal crystal templating, J. Colloid. Interface. Sci., 316 (2007) 547–552.
[3] R. Takagi, K. Masui, S. Nakamura, T. Tsujioka, Metal patterning using maskless vacuum evaporation process based on selective deposition of

photochromic diarylethene, Appl. Phys. Lett., 93 (2008) 213304.
[4] P. Dunne, J.M.D. Coey, Patterning metallic electrodeposits with magnet arrays, Phys. Rev. B - Condens. Matter Mater. Phys., 85 (2012) 1–21. doi:10.1103/PhysRevB.85.224411:32
[5] K. Tschulik, R. Sueptitz, J. Koza, M. Uhlemann, G. Mutschke, T. Weier, A. Gebert, L. Schultz, Studies on the patterning effect of copper deposits in magnetic gradient fields, Electrochim. Acta, 56(1) (2010) 297-304.
[6] F. Karnbach, M. Uhlemann, A. Gebert, J. Eckert, K. Tschulik, Magnetic field templated patterning of the soft magnetic alloy CoFe, Electrochim. Acta, 123 (2014) 477-484.
[7] J. R. Chiou, B. H. Lai, K. C. Hsu, D. H. Chen, One-pot green synthesis of silver/iron oxide composite nanoparticles for 4-nitrophenol reduction, J. Hazard. Mater., 248 (2013) 394-400.
[8] M. Sathishkumar, K. Sneha, S. W. Won, C.W. Cho, S. Kim, Y.S.Yun, Y.S., Cinnamon zeylanicum bark extract and powder mediated green synthesis of nano-crystalline silver particles and its bactericidal activity, Colloid Surface B, 73(2) (2009) 332-338:
[9] Z. Sun, F. Su, W. Forsling, P. Samskog, Surface Characteristics of Magnetite in Aqueous Suspension, J. Colloid Interface Sci., 197(1) (1998) 151-159 doi:10.1006/jcis.1997.5239.

Figures 1. (a) – the schematic comparison of standard selective metallisation process (left) and the modified method (right), (b) – the set-up of magnet attachment.

Bill Wilkie's Notes

Bill Wilkie
Technical Director and Organiser

Some of our older members are privileged to have been with the PCB Industry since its infancy.

In the early days, communication was by letter, then fax and now almost all by email. Although social media has been in use for some time, we (the Institute) are only just beginning to receive information, mainly from LinkedIn, but also on Facebook. Sometimes the information is unintended, as we can see from 'Anniversaries' that the Member has moved to a different Company and sometimes intentional, when a Member gets in touch to pass on some news, when they are already on LinkedIn.

At our last evening seminar at Harrogate, I was able to say a few words about the campaign to stop the banning of Fluorine via our members on BSI Committees and ask that after they'd logged out of LinkedIn and finished with Facebook, that they log on to our website.
I requested that they look at the newsfeeds and the BSI page and see what the ICT/BSI are doing on behalf of our Industry. It might not seem important at the time, but the vigilance of the ICT/BSI committee members may have prevented far reaching malfeasance based on nothing more than an element's position on the periodic table.

ICT Members on BSI Committees

Len Pillinger
Dennis Price
Emma Hudson
Andy Critcher

Bill Wilkie

Technical Director and Organiser

Corporate Members of The Institute of Circuit Technology January 2018

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