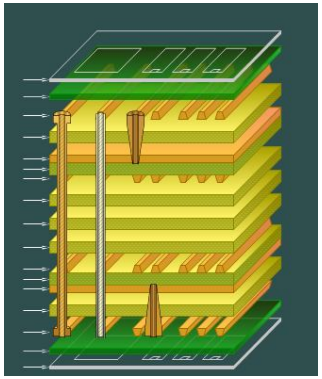
Calculating Specifying and Testing Electrical Characteristics of PCB's

Sept 2010



Neil Chamberlain

European Sales Manager

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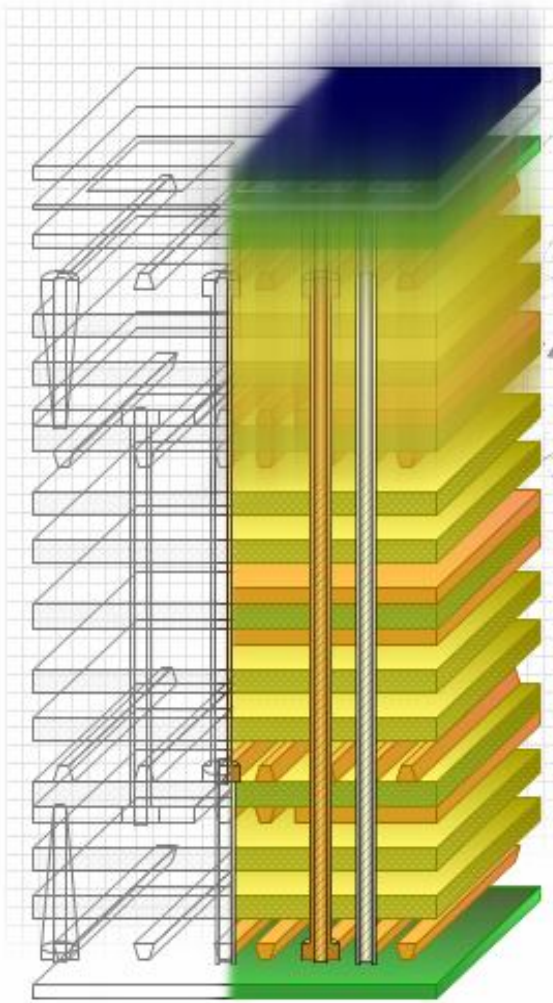


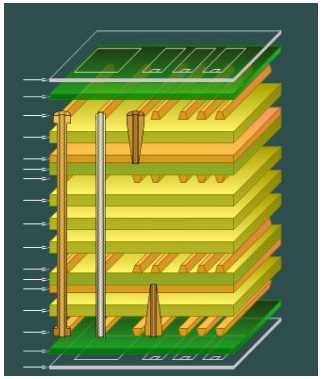
Speedstack PCB

Automatic impedance controlled
PCB stackup design & documentation

Polar Instruments

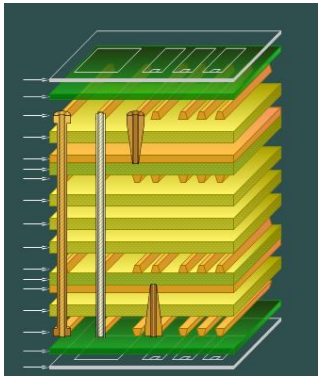
Agenda

- Why Controlled Impedance
- Calculating Impedance
  - Modelling
  - FR4 Issues
- Specify Impedance
  - Correct Calculations
  - Correct Documentation
- Testing Impedance
  - Coupon Design
  - TDR Testing
  - Testing for Loss



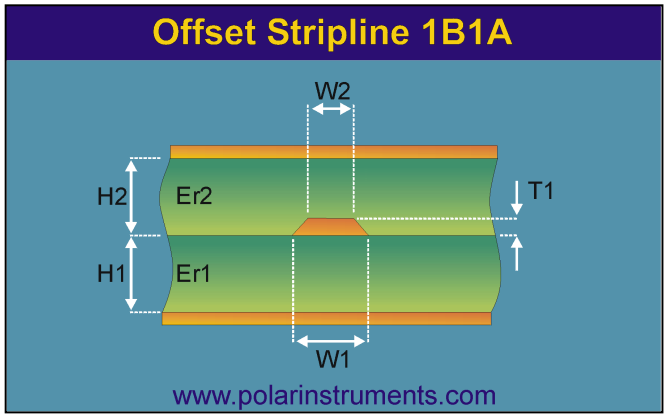
Why Impedance Matching

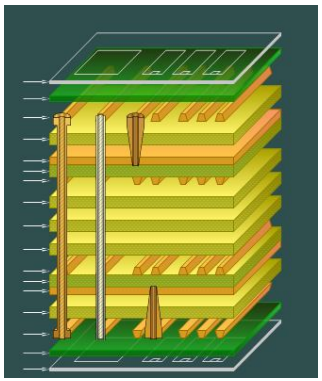
- Controlling Signal Noise
- Signal Termination
  - Xaui
  - Rocket I/O
- Specification
  - USB 2
  - PCi Express
  - DDr 3
- RF Filtering



Accurate Impedance Calculation

- Simulate Trace Geometries
- Use Accurate Model

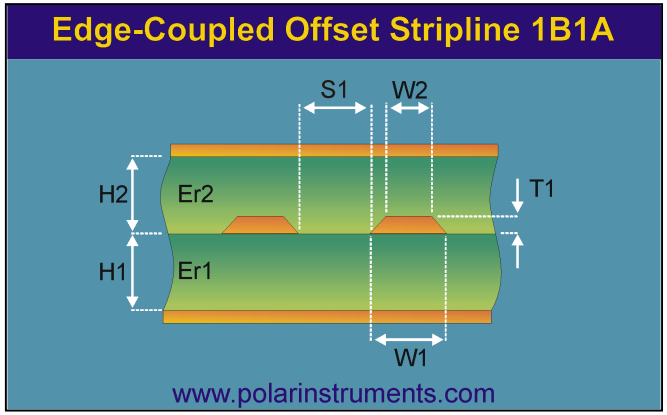


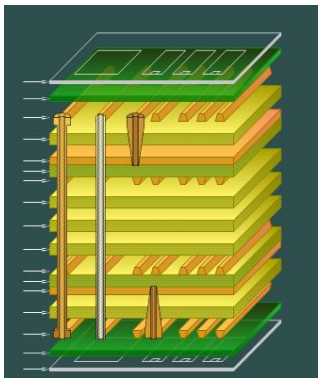


- Requires a 2d Field solver

Trapezoidal Model

- Two input parameters required for Trace Width
- Models the Print and Etch process within the PCB Manufacture

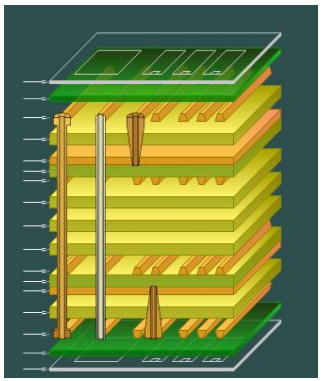


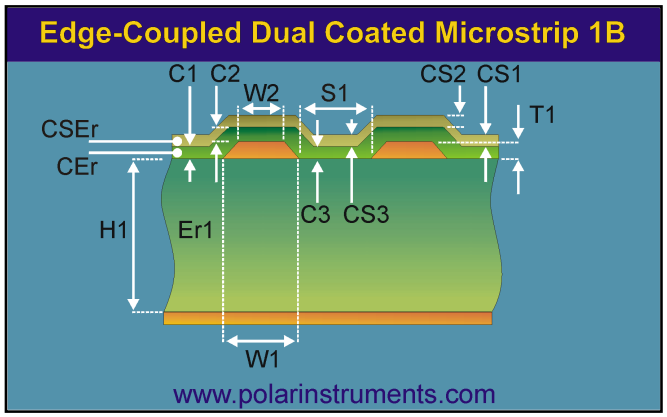


•These numbers can be provided by your PCB Manufacture

Solder Mask Modelling

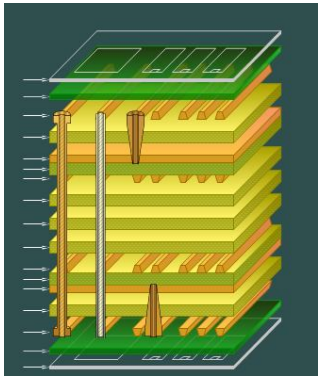
- Solder mask has a large effect on impedance on surface traces
- Depending on Geometry can be as large as 5Ω

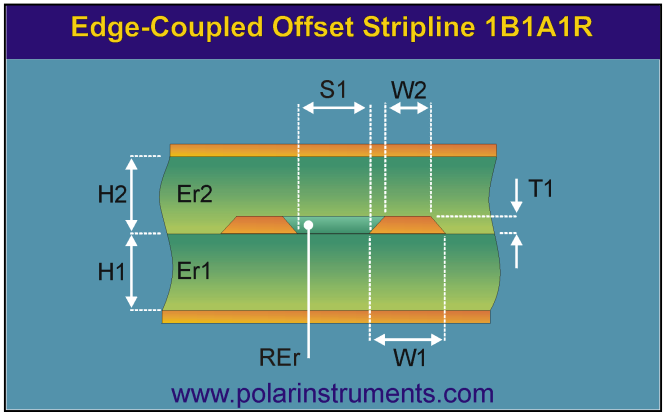




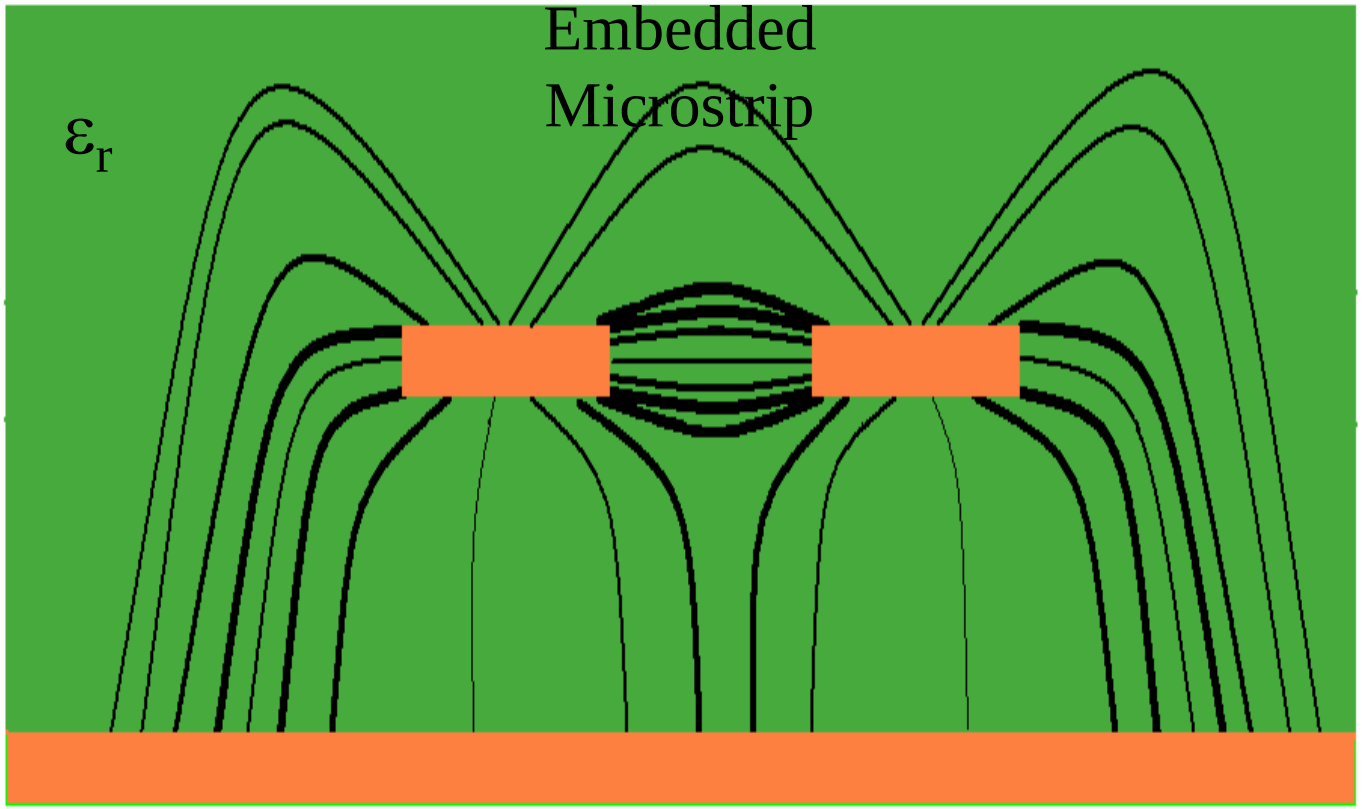
Resign Modeling

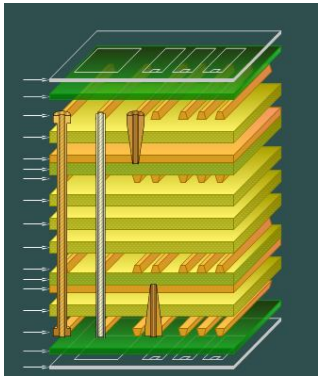
- Both are Mixtures of Resin and Glass Fibers
  - Materials are non-homogenous
    - ε_r specified for laminate is the bulk value
    - ε_r for glass ~ 6.1 ε_r for epoxy ~ 3.2
  - So significant local variations occur for ε_r



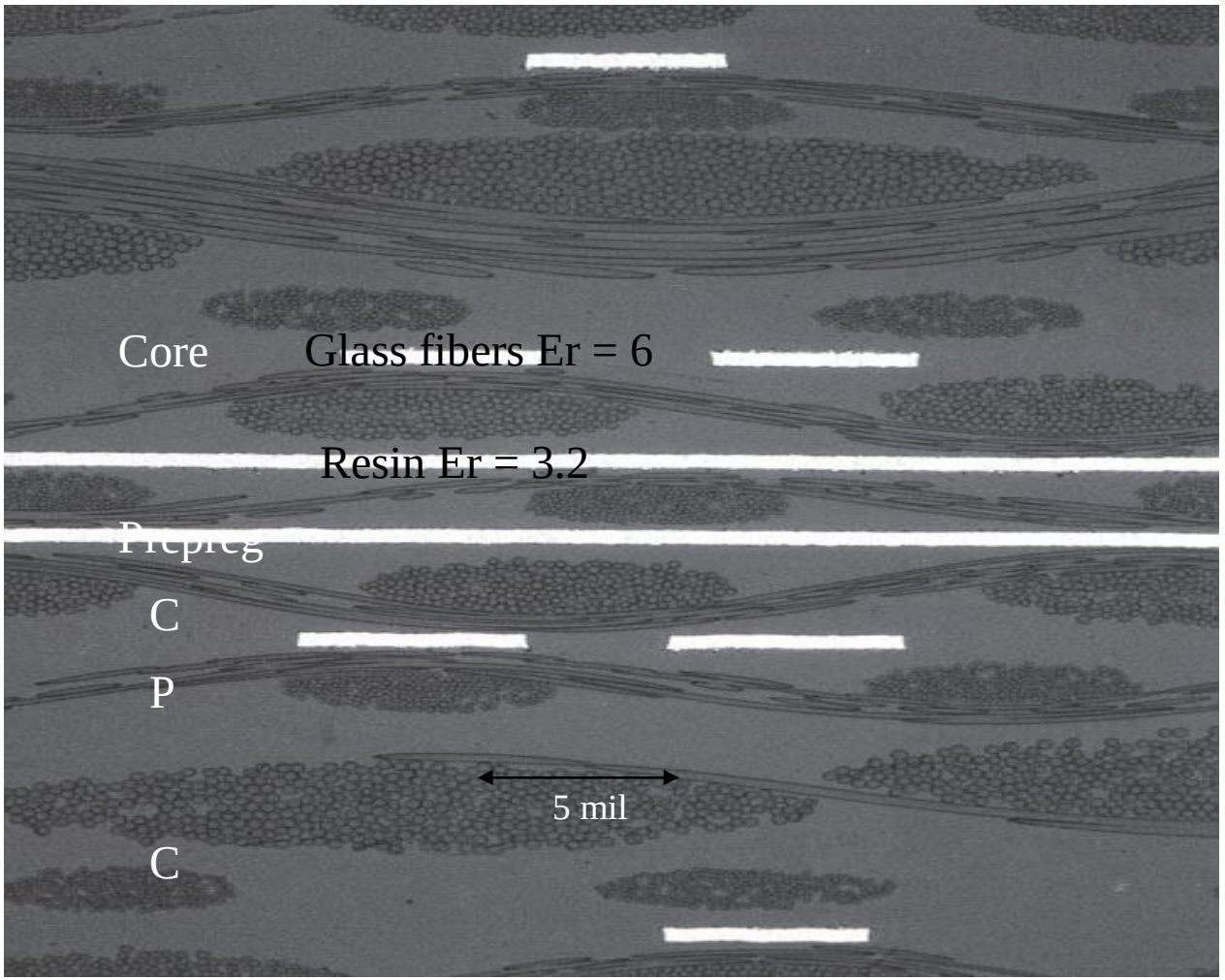


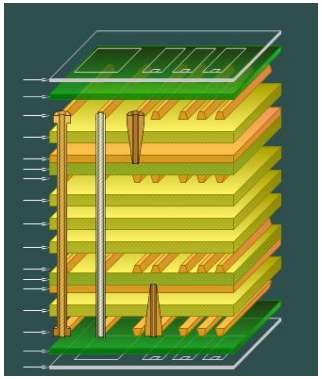
Typical E-field distribution





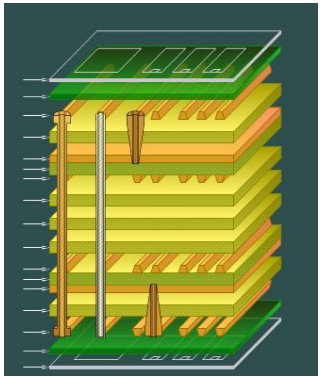
Microphotograph of FR4 structure

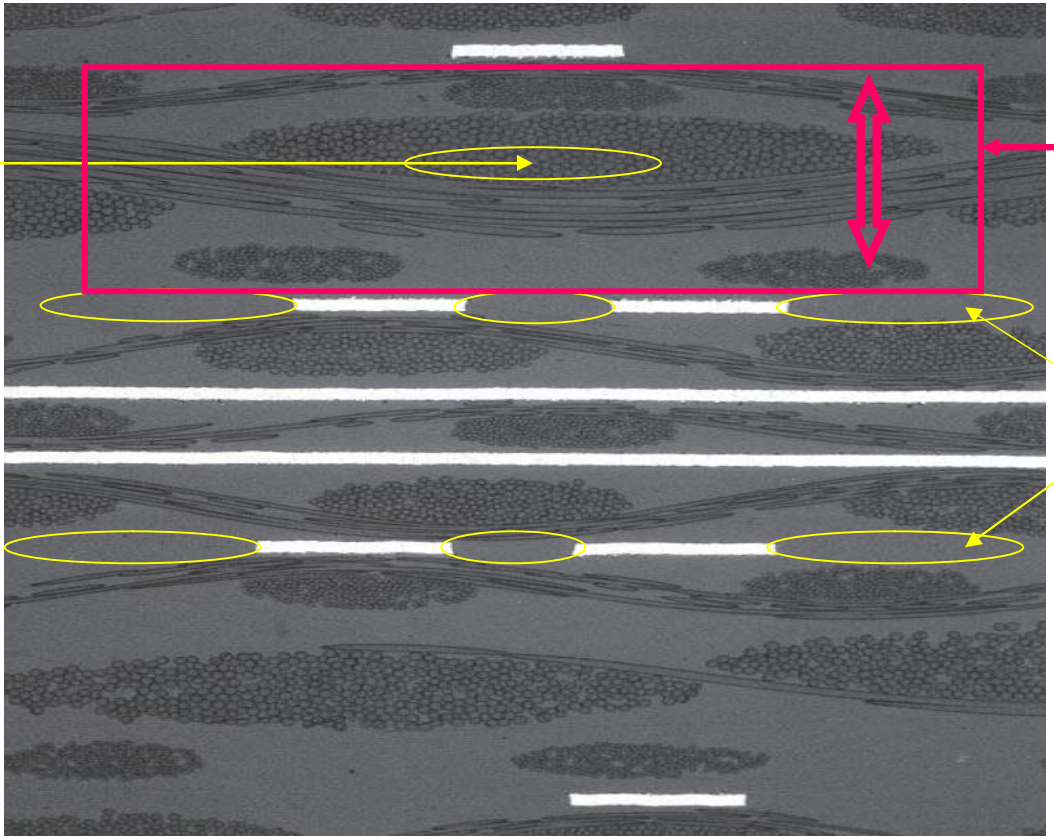




FR4 structure

Er = 6.0

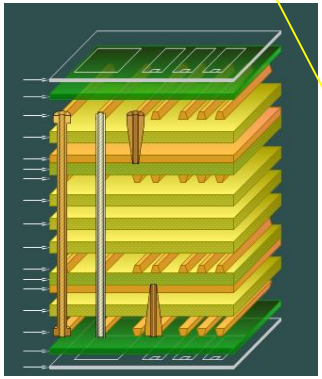


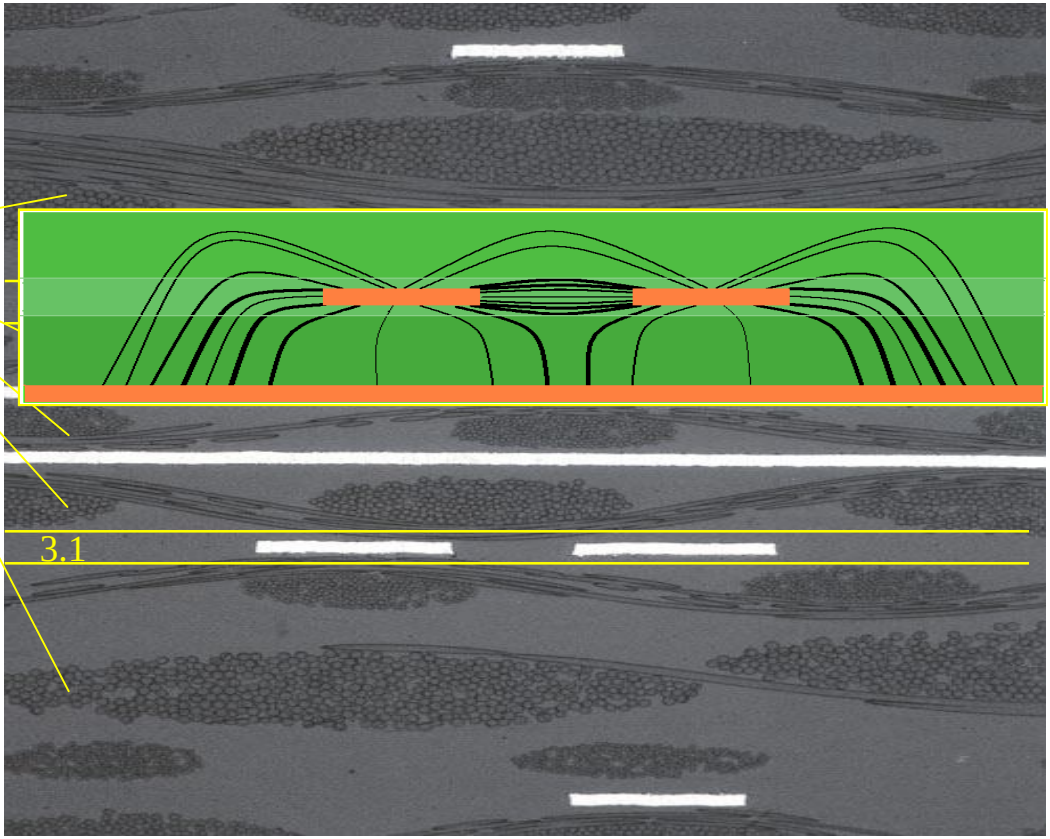


Bulk Er value in this direction is 4.2 approx

Er = 3.2

Field in FR4 structure



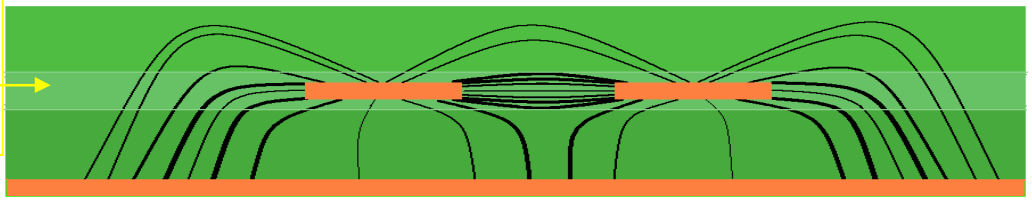


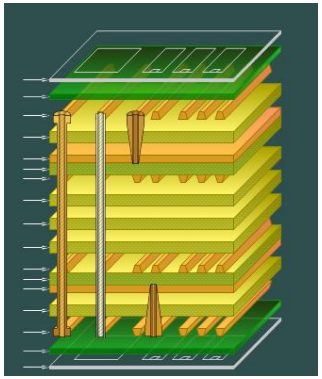
Field distribution in Differential Pair

Impedance value

Increases as

Er and C decrease

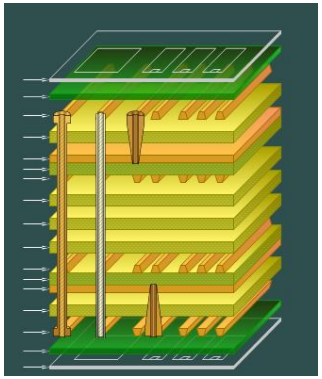




All Models are Wrong

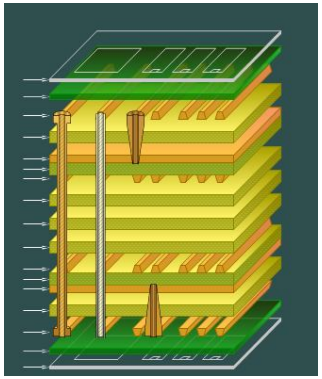
But Some are Useful !!

Tolerance needs to be given on all Simulated results

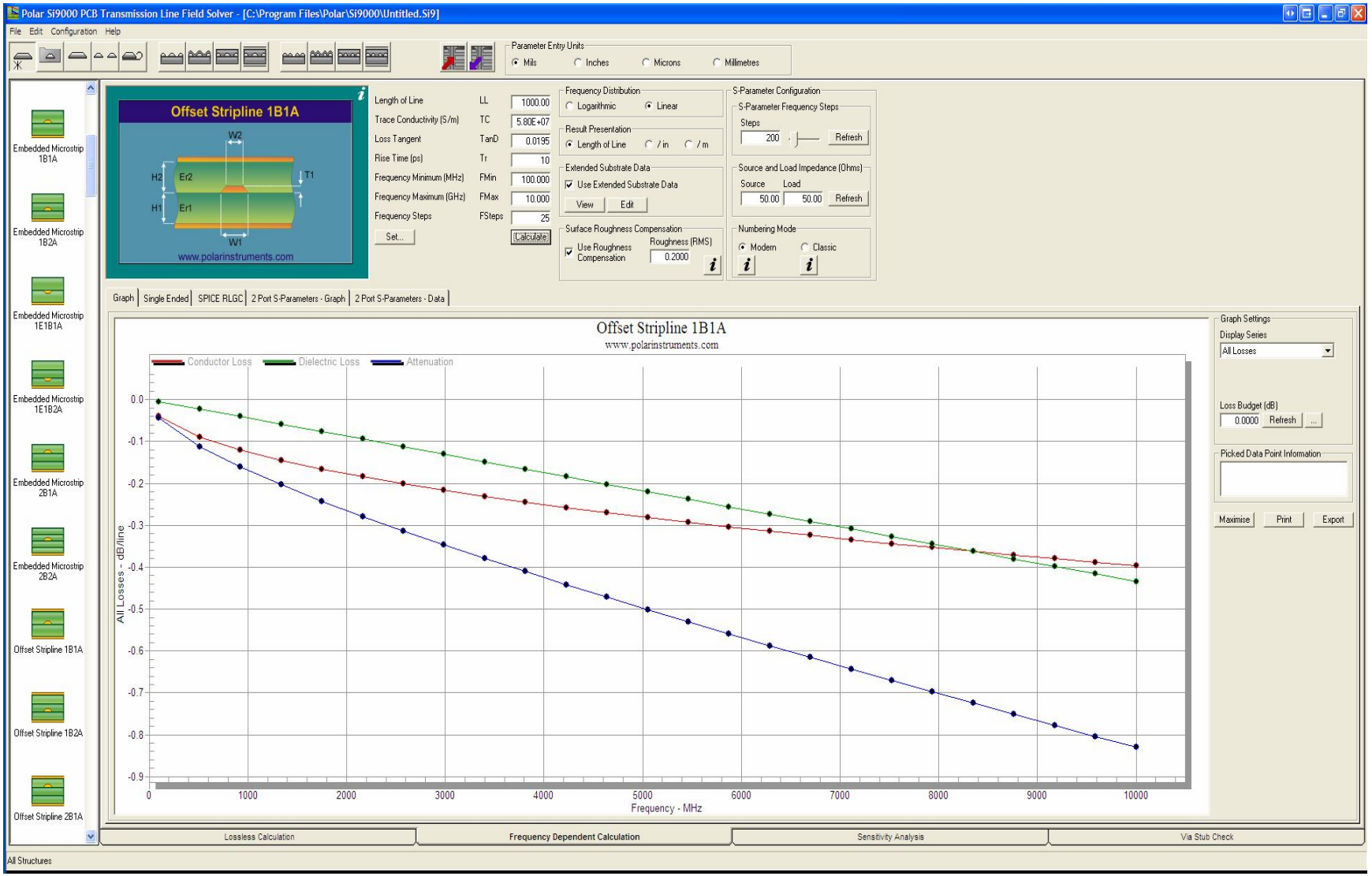


Modelling Losses

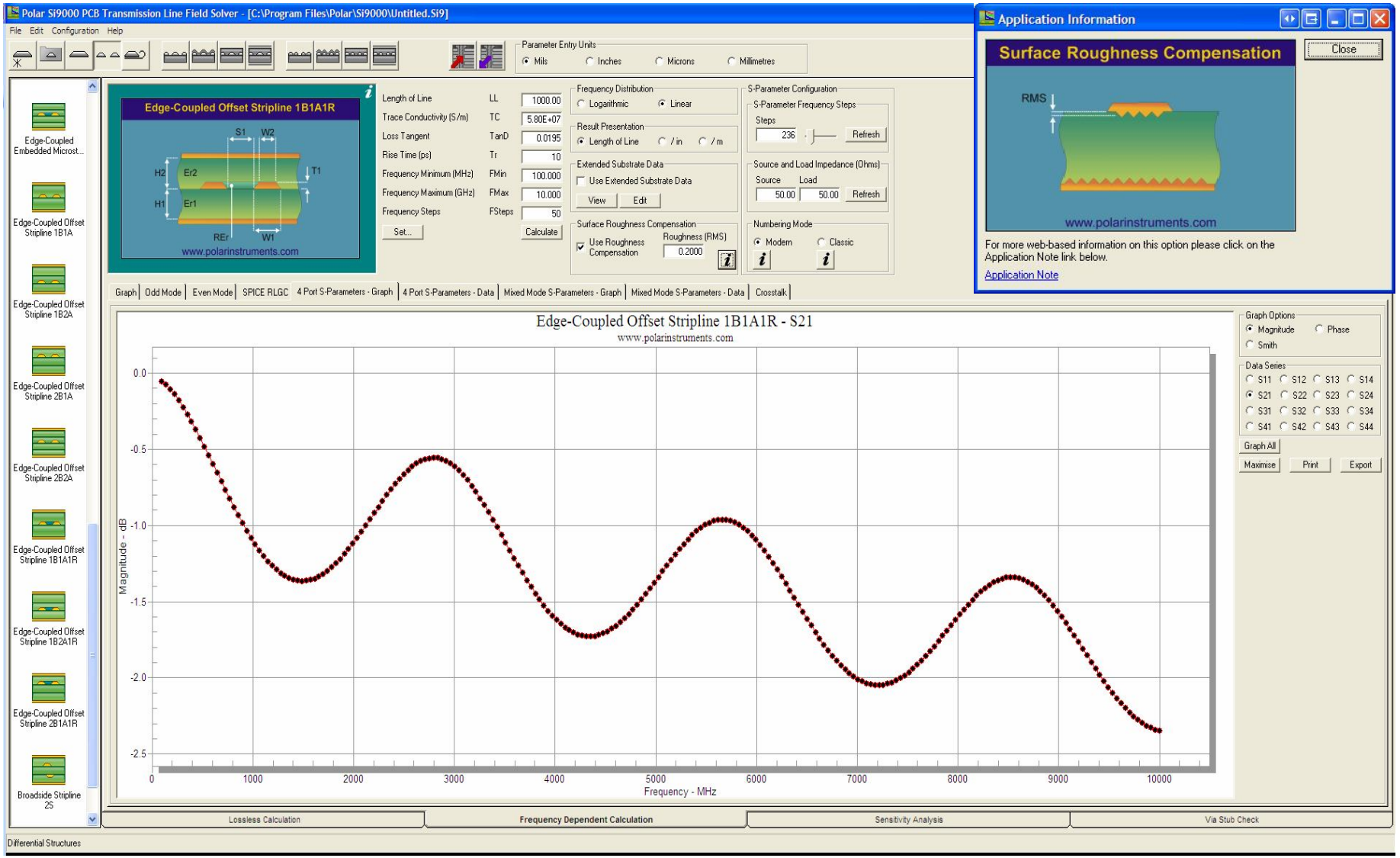
- Designers need to concern themselves with Loss as well as Impedance
- Frequency Dependant Modelling
- Low Dk Material Modelling



Modelling Loss

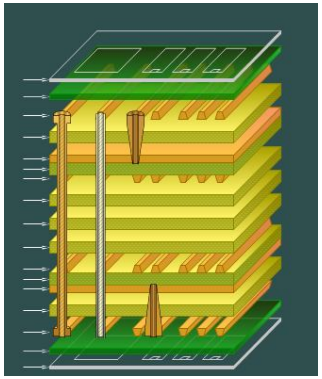


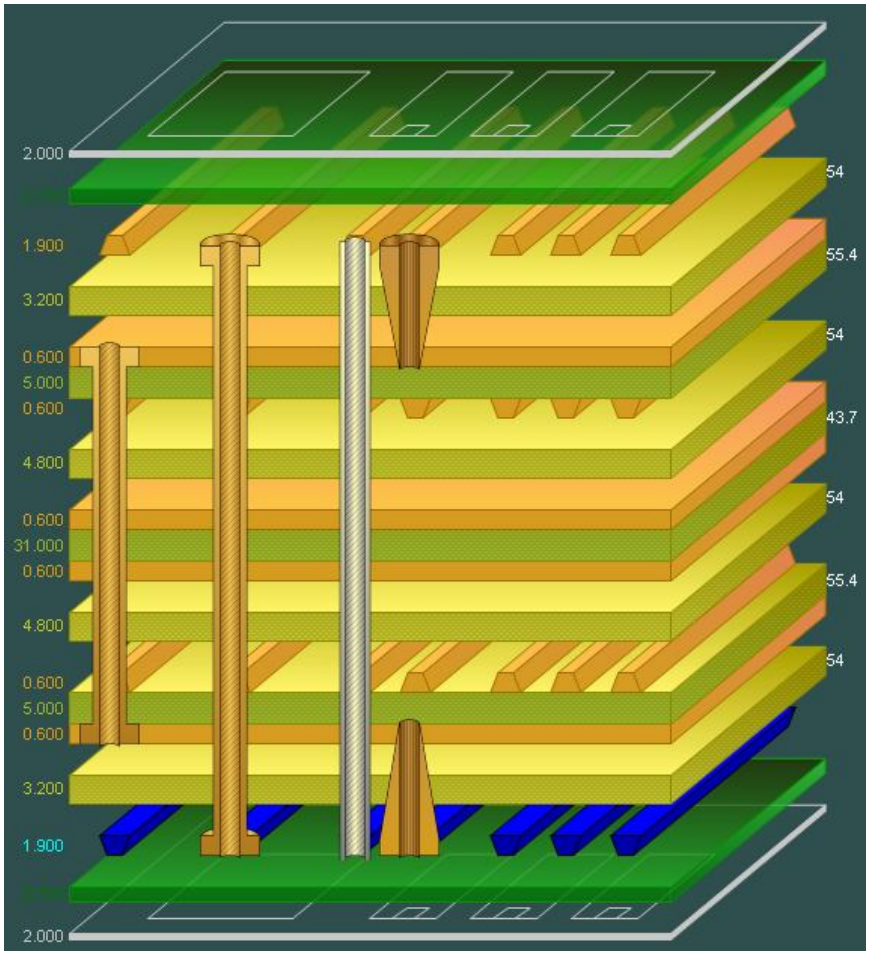
Modelling Loss



So How do we get the modelled results to the fabricator

Document your stacks like this:





And like this:

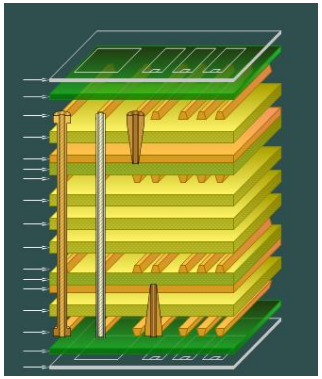
Layer	Stack up	Supplier	Supplier Description	Impedance ID	Description	Processed Thickness	εr	Data Filenames
	Primary							
		Polar Samples	PE/001		Peelable Mask			Primary-Side-Peelable-P1.ger
		Polar Samples	ID/001		Screened Ident			Primary-Side-Ident-I1.ger
		Polar Samples	SM/001		Liquid PhotoImageable Mask		4.00	Primary-Side-Solder-Mask-S1.ger
1		Polar Samples	FO/001	1	Copper Foil	1.40		Primary-Side-L1.ger
		Polar Samples	PP/001		PrePreg 1080	2.79	4.20	
2						1.40		Ground-Plane/Inner-Tracking-L2.ger
		Polar Samples	CO/020		FR4 Core	12.00	4.20	
3				2		1.40		Inner-Tracking-L3.ger
		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	
		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	
4						1.40		3V3-Power-Plane-L4.ger
		Polar Samples	CO/017		FR4 Core	8.00	4.20	
5						1.40		1V5/2V5-Power-Plane-L5.ger
		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	
		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	
6						1.40		Inner-Tracking-L6.ger
		Polar Samples	CO/020		FR4 Core	12.00	4.20	
7				3		1.40		Ground-Plane/Inner-Tracking-L7.ger
		Polar Samples	PP/001		PrePreg 1080	2.79	4.20	
8		Polar Samples	FO/001	4	Copper Foil	1.40		Secondary-Side-L8.ger
	Secondary	Polar Samples	SM/001		Liquid PhotoImageable Mask		4.00	Secondary-Side-Solder-Mask-S8.ger

63 +10% / -10%

Copper Thickness = 11.200 | Dielectric Thickness = 51.340 | Overall Processed Thickness = 62.540

Notes

Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Trace Separation	Ground Strip Separation	Lower Ground Strip Width	Calculated Impedance	Target Impedance	Tol (+/- %)
1	Coated Microstrip 1B	1	2	0	4.25	0.00	0.00	0.00	49.38	50.00	10.00
2	Offset Coplanar Strips 1B1A	3	2	4	19.00	0.00	8.00	15.00	27.84	28.00	10.00
3	Diff Embedded Coplanar Waveguide With Lower Ground 1B1A	7	5	0	12.00	8.50	27.00	0.00	100.57	100.00	10.00
4	Coated Microstrip 1B	8	5	0	20.00	0.00	0.00	0.00	75.30	75.00	10.00



StackName: 8-Layer Sample Stack	Version: A	Revision:	Modification:	Date of Revision:	Editor		
Date: 17/06/2006	Associated Documents:	2	3113 swp to 108	31/3/09	JAS	Page 1/1	Speedstack 2009
Author: James Stapley							
Department: Engineering							
Site: Waterlooville							

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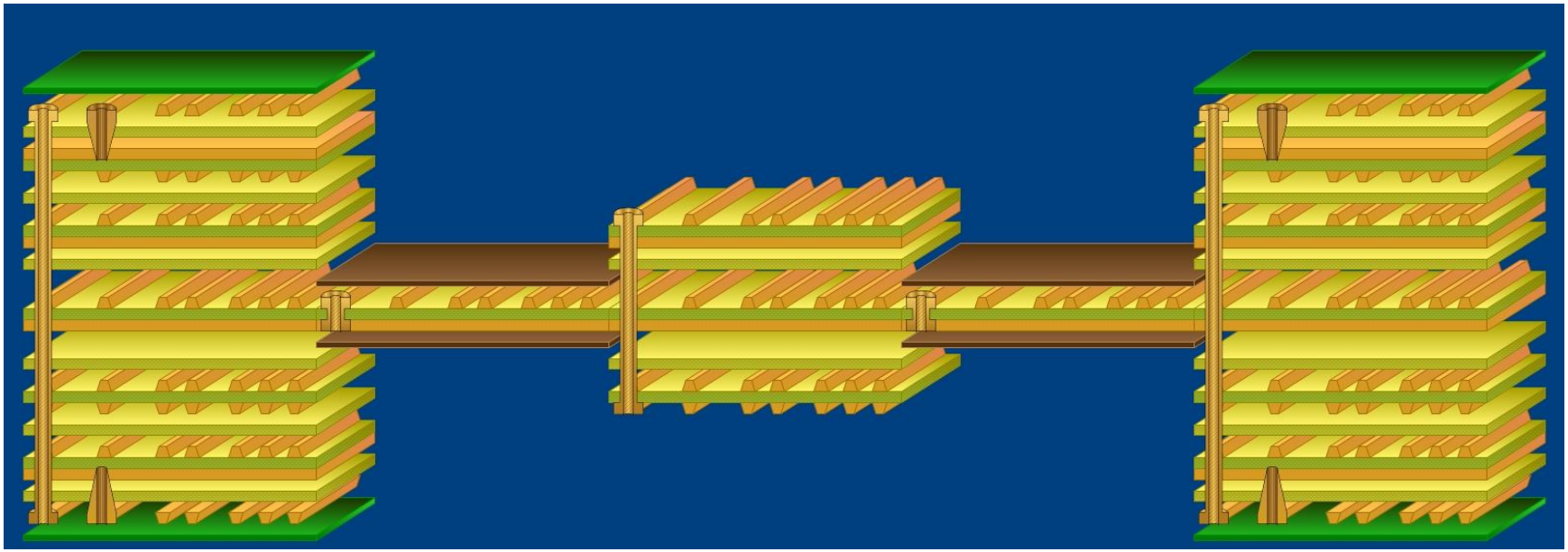
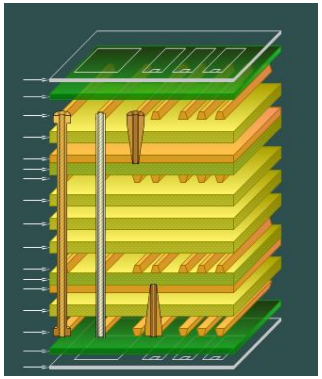
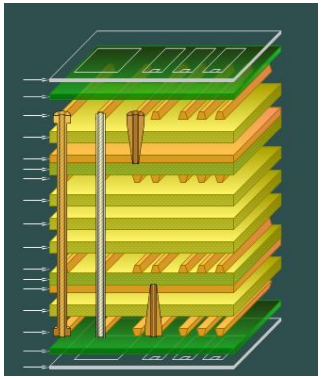
Even Document Flex Rigids Like this:





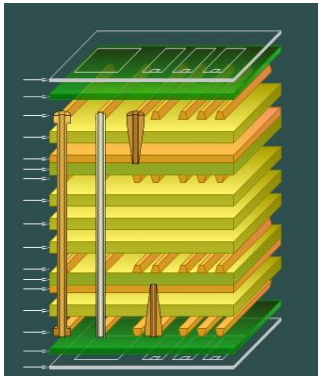
Why is stackup design and communication important?

- Time to market
- Complex designs
- Communication from designer to PCB fabricator
- Increasing impedance requirements
- Can be time consuming
- Good communication saves costly rebuilds

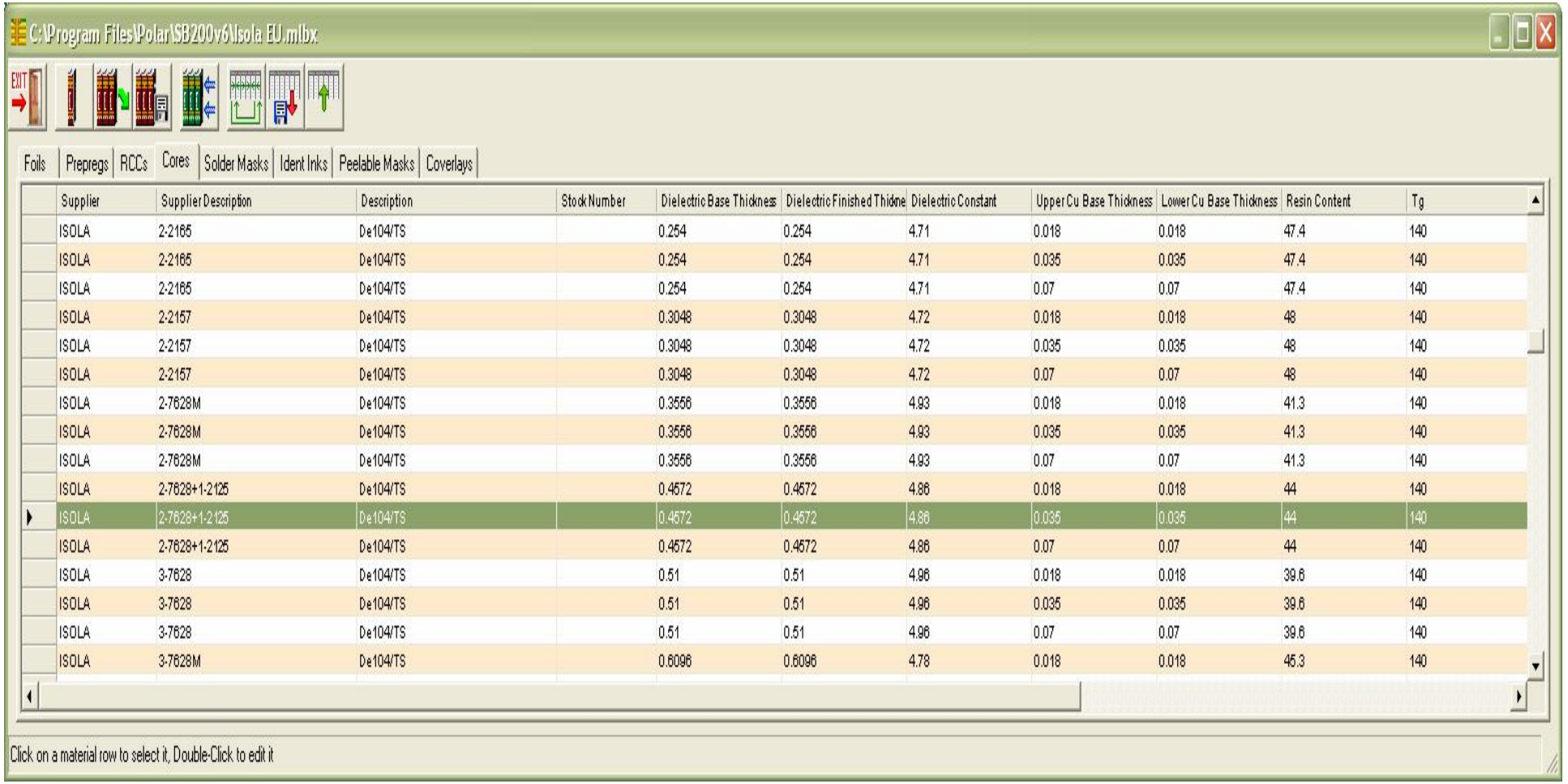


Material Libraries

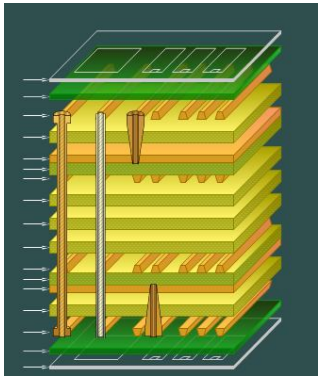
- Based on the parameters of actual material.
- Separated into material types
  - Cores
  - Prepregs
  - Foils, etc.

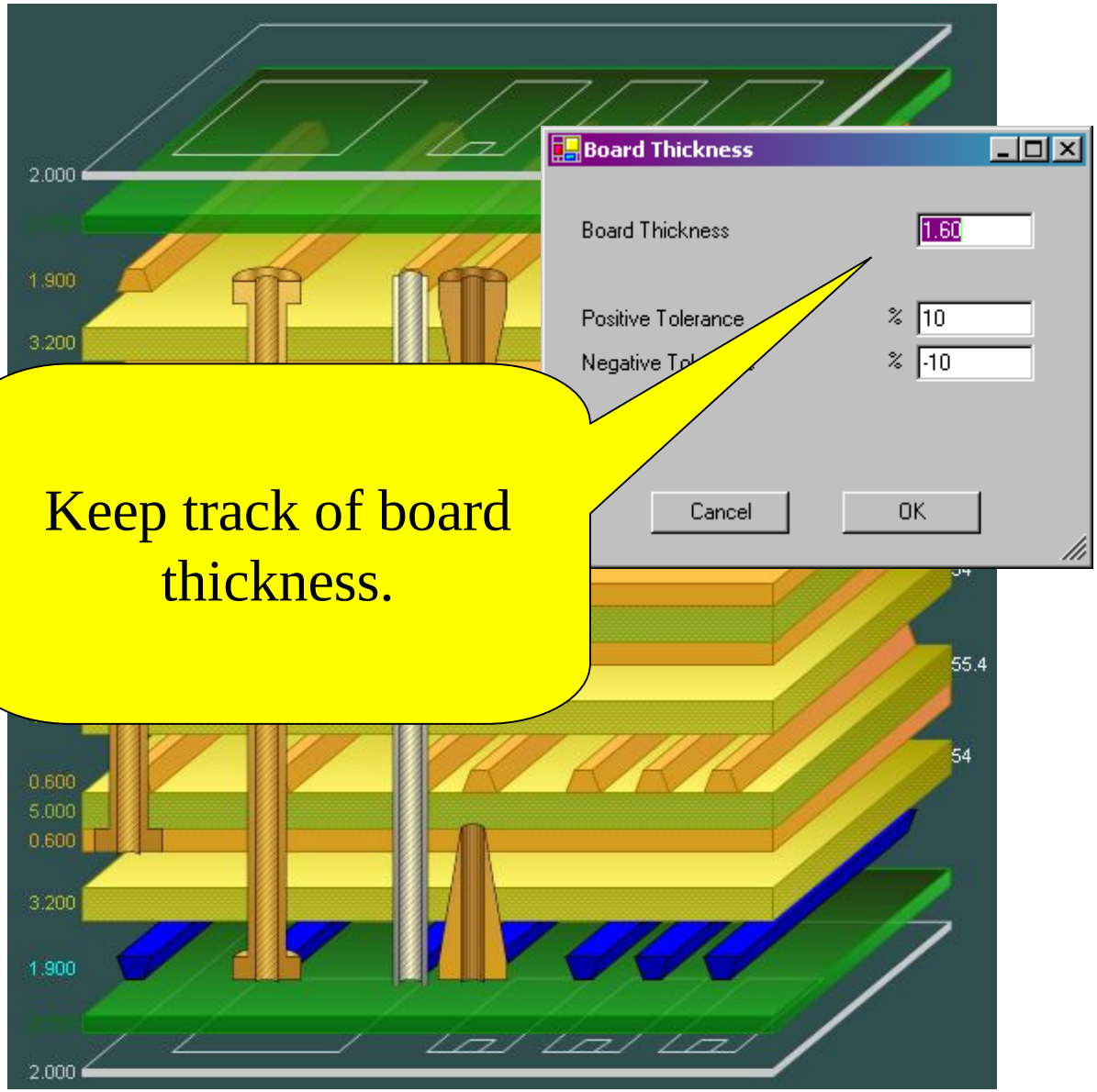


The info required for cores



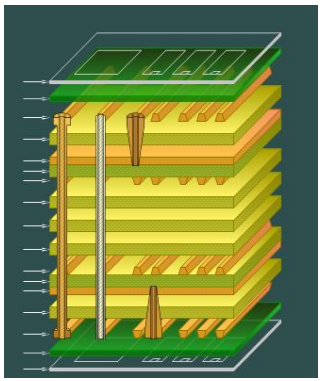
Will it fit?!!

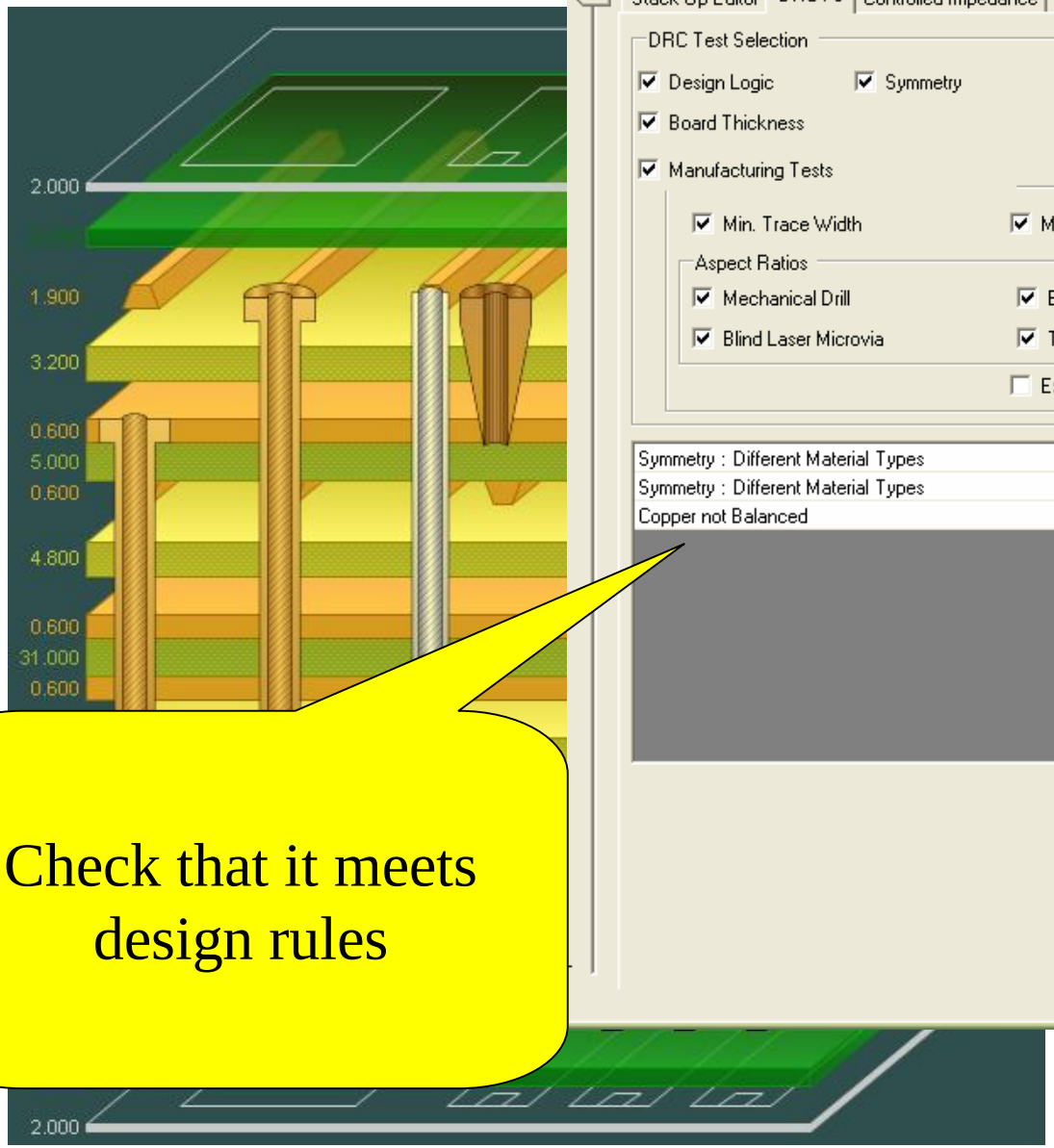




Keep track of board thickness.

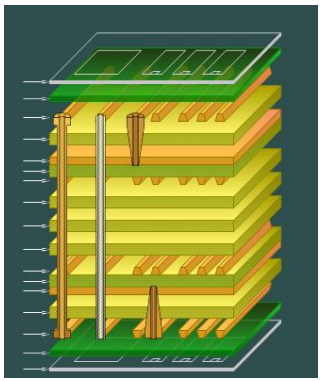
D.R.C.

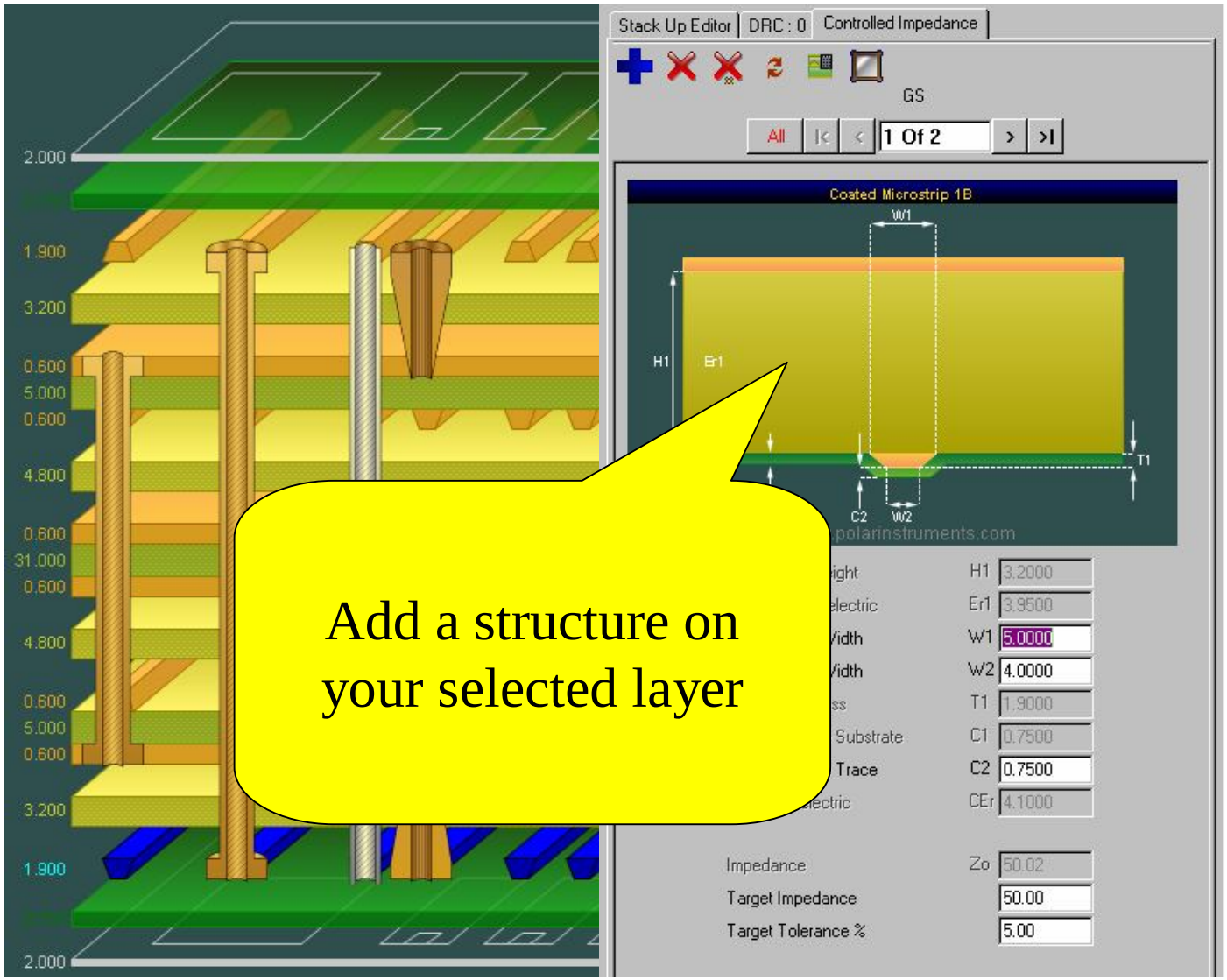




Check that it meets design rules

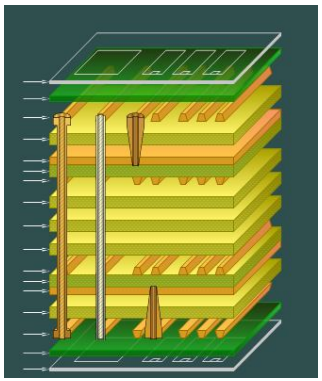
Adding a controlled impedance structure

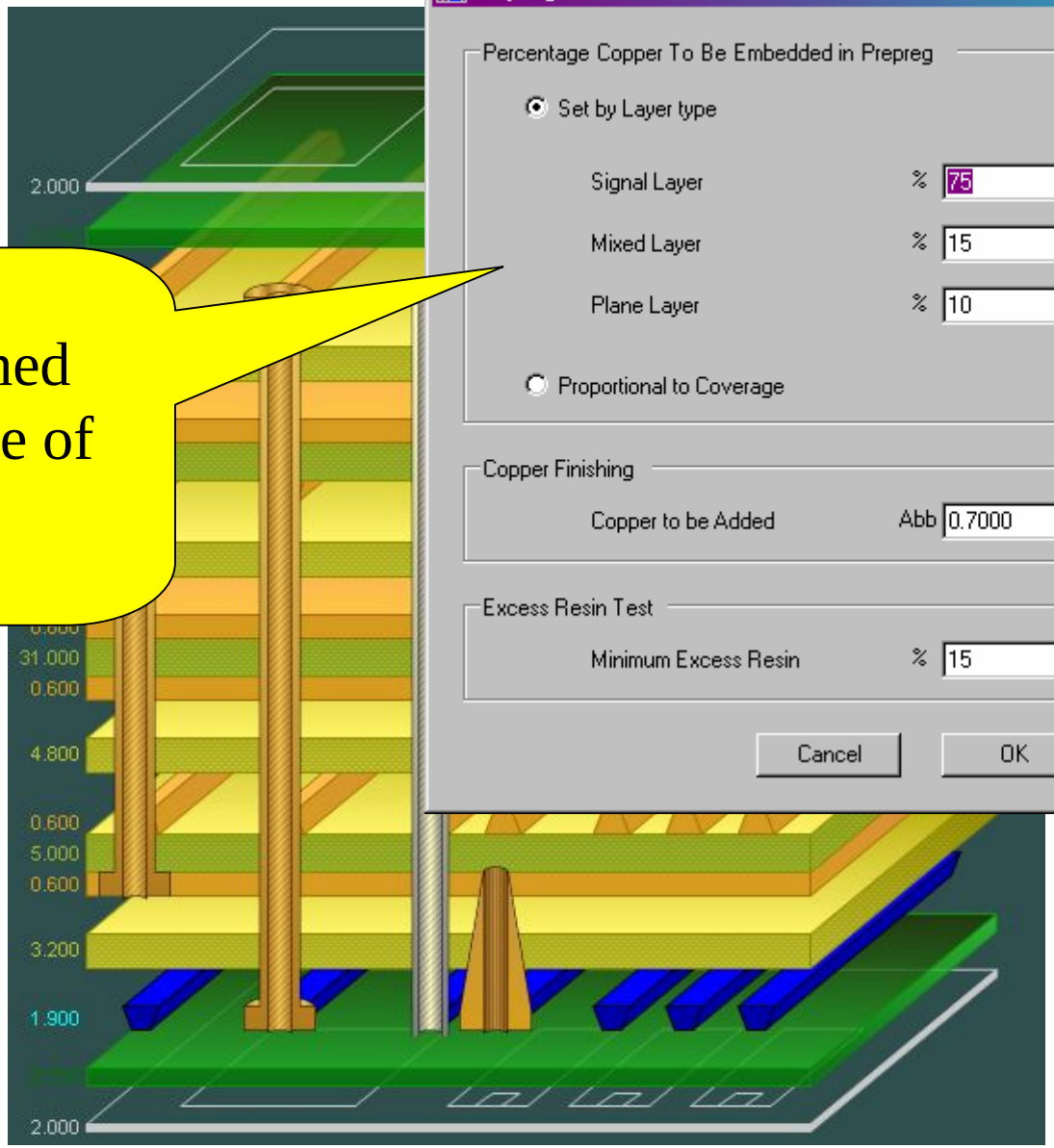




Finished thickness calculation:

Calculate finished thickness (choice of methods).





Prepreg Corrections

Percentage Copper To Be Embedded in Prepreg

Set by Layer type

Signal Layer % 75

Mixed Layer % 15

Plane Layer % 10

Proportional to Coverage

Copper Finishing

Copper to be Added Abb 0.7000

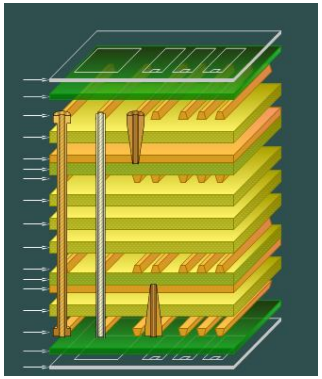
Excess Resin Test

Minimum Excess Resin % 15

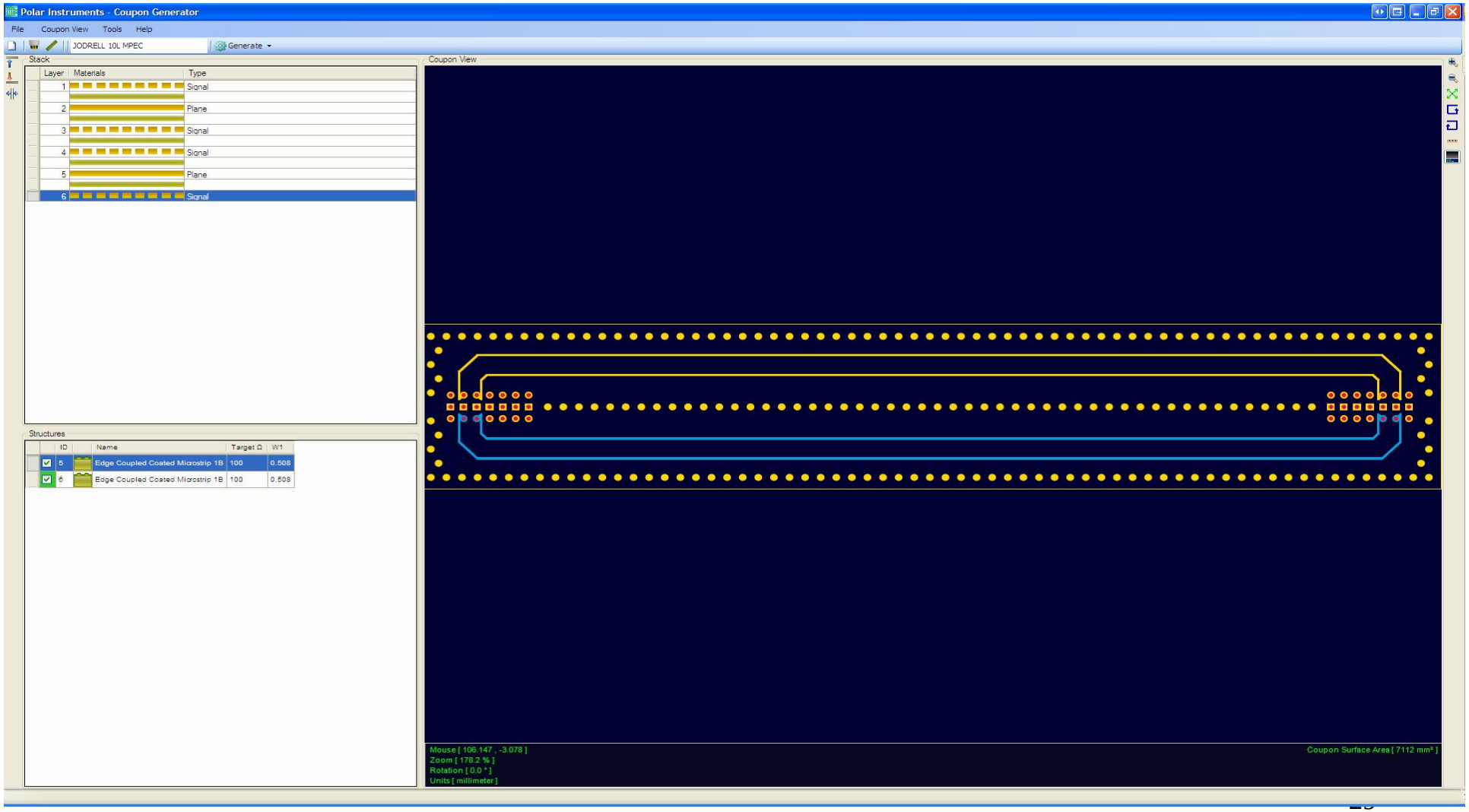
Cancel OK

Drill documentation:

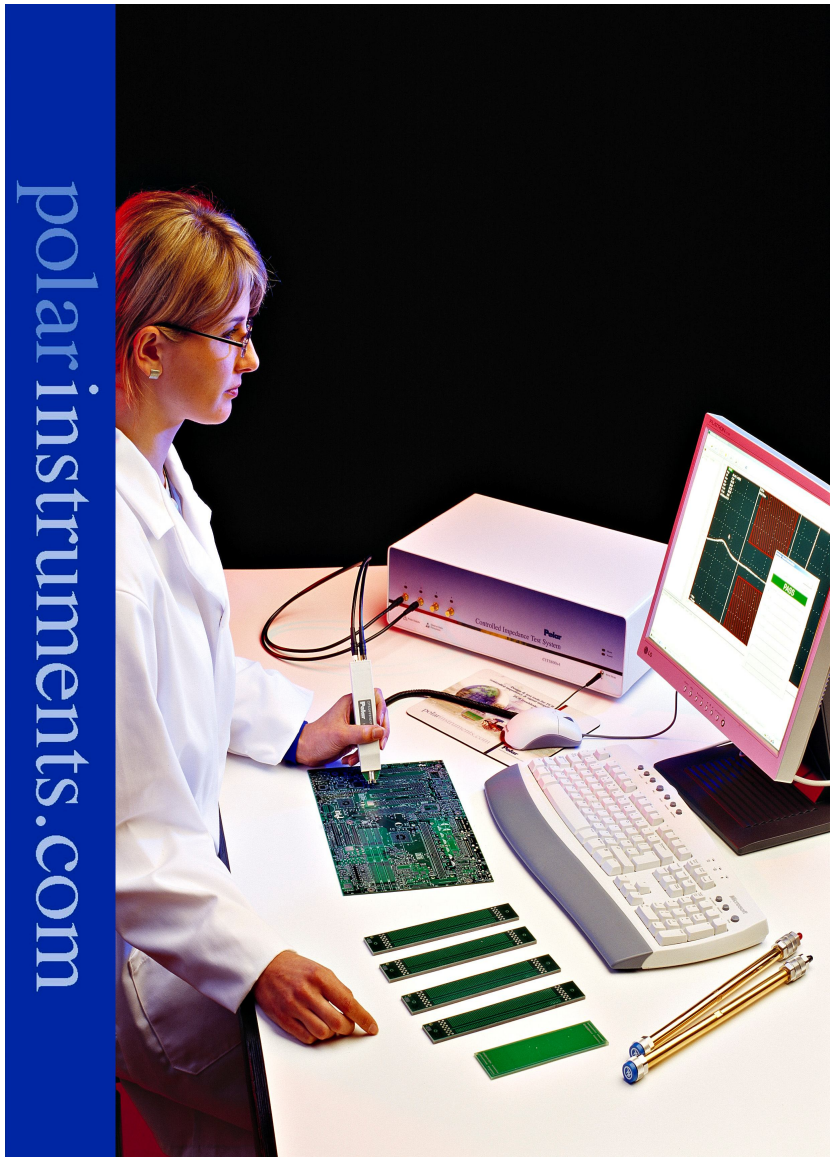
Document conventional laser blind buried and stacked vias.



Coupon Testing



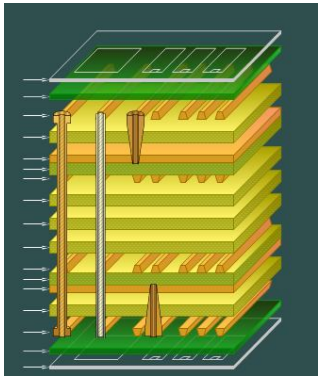
TDR Testing



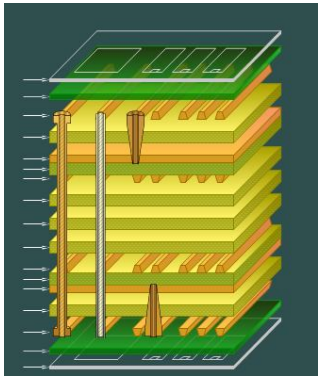
- Testing is not difficult or Time consuming
- Required for Process conformance to Specification.
- MVT not DVT.

The Future of testing:- Atlas

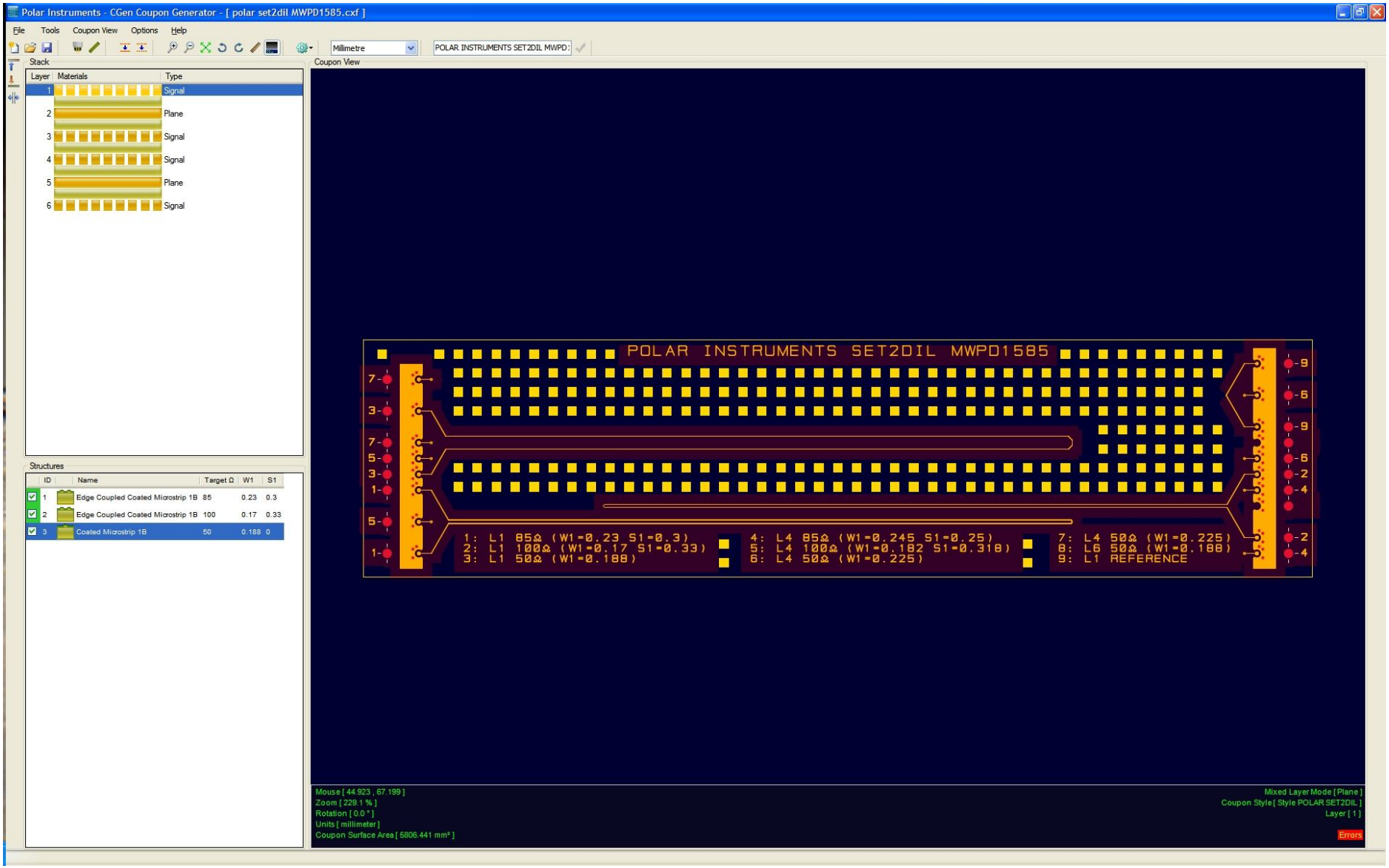
- New high speed busses in Multi GHz range
  - SuperSpeed USB 3.0
  - PCI Express Gen 2.0
- Differential Signalling techniques allow the continued uses of FR4
- Requires accurate control of tranmission line losses



The Future of testing:- Atlas

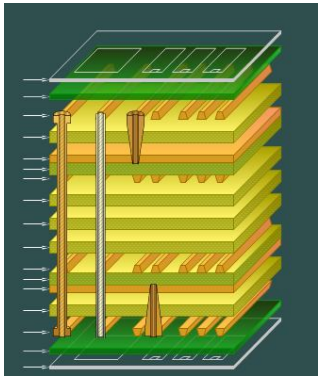


Atlas Coupon Test



Conclusion

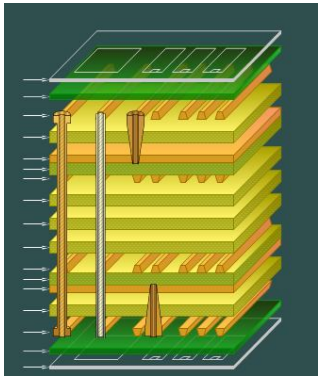
- Accurate Modelling is as important as final testing.
- Material selection is critical to the performance of the final product
- Clear Documentation is imperative
- Testing final product is made easy through robust test system.



Thank You

- Questions?….

  Neil@polarinstruments.com



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