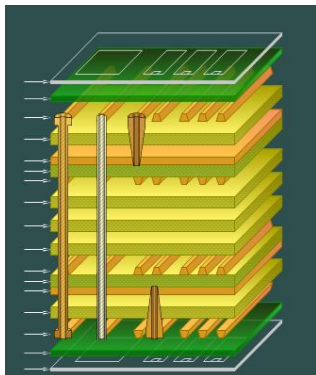


Calculating Specifying and Testing Electrical Characteristics of PCB's

Sept 2010



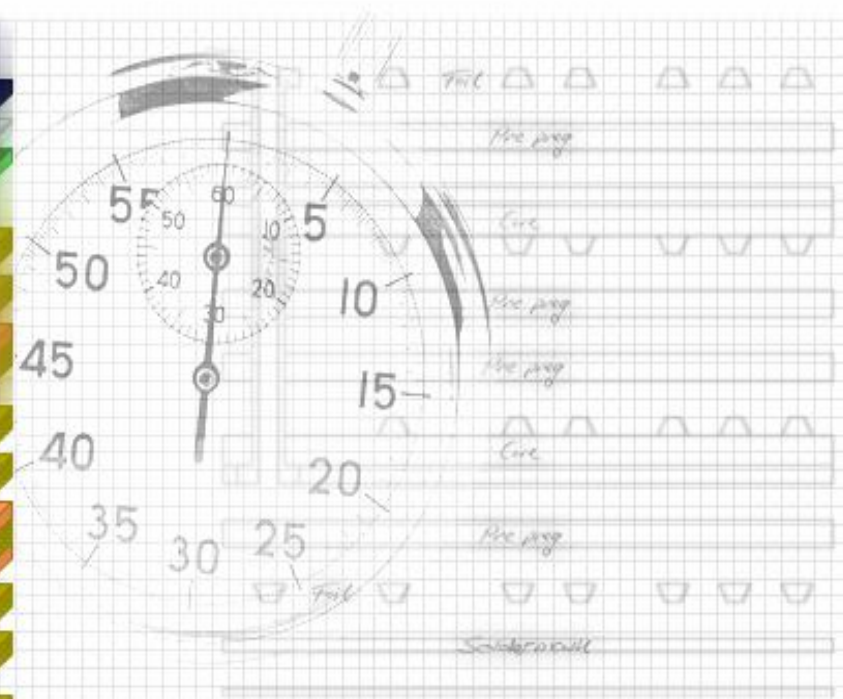
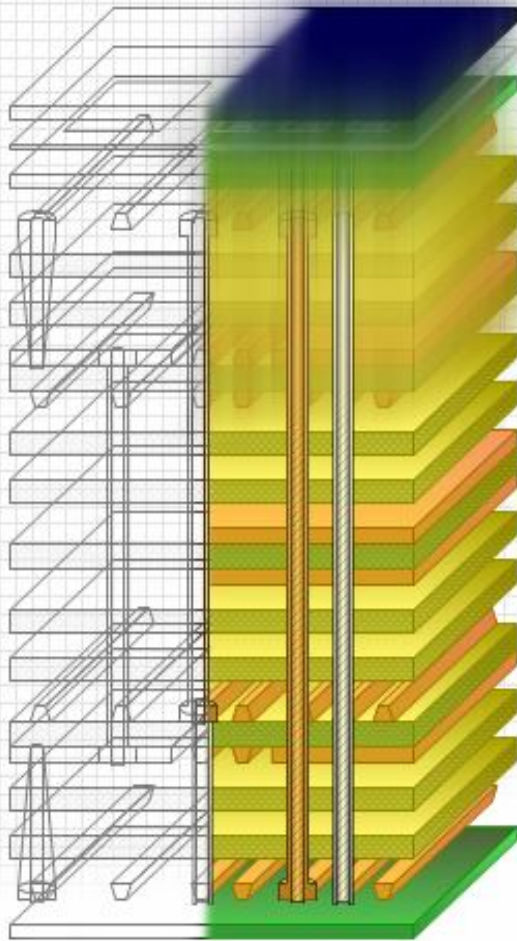
Neil Chamberlain

European Sales Manager

www.polarinstruments.com



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Speedstack PCB

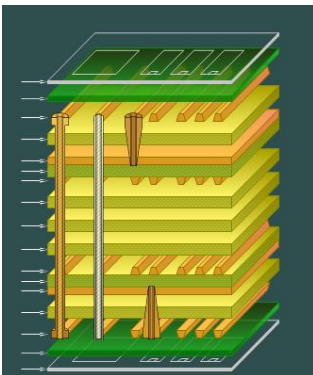
Automatic impedance controlled
PCB stackup design & documentation

Polar Instruments



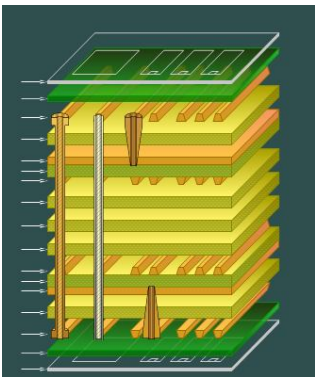
Agenda

- Why Controlled Impedance
- Calculating Impedance
 - Modelling
 - FR4 Issues
- Specify Impedance
 - Correct Calculations
 - Correct Documentation
- Testing Impedance
 - Coupon Design
 - TDR Testing
 - Testing for Loss



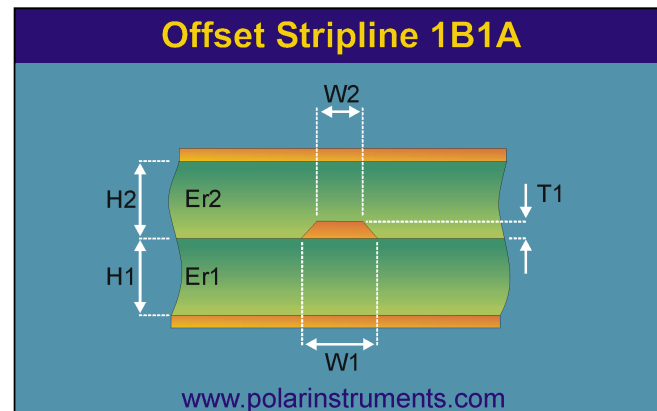
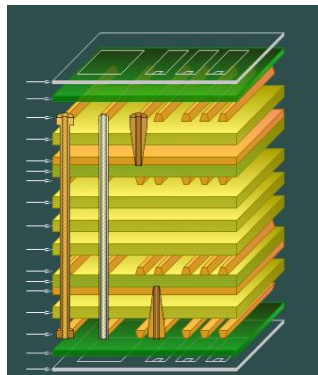
Why Impedance Matching

- Controlling Signal Noise
- Signal Termination
 - Xaui
 - Rocket I/O
- Specification
 - USB 2
 - PCi Express
 - DDr 3
- RF Filtering



Accurate Impedance Calculation

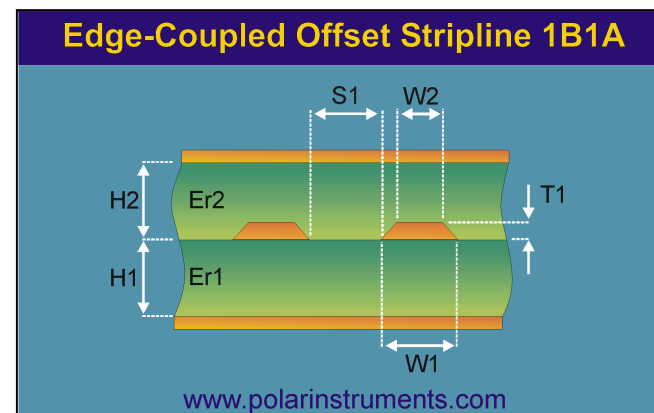
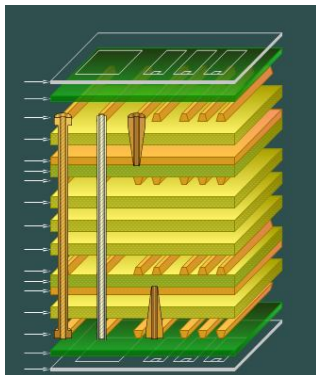
- Simulate Trace Geometries
- Use Accurate Model



- Requires a 2d Field solver

Trapezoidal Model

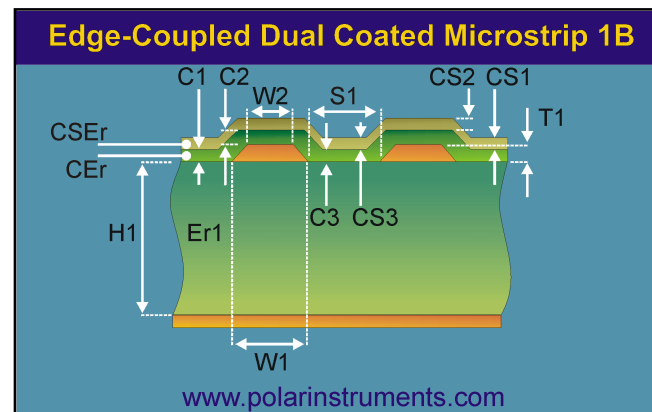
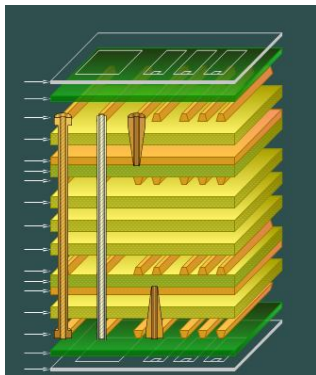
- Two input parameters required for Trace Width
- Models the Print and Etch process within the PCB Manufacture



- These numbers can be provided by your PCB Manufacture

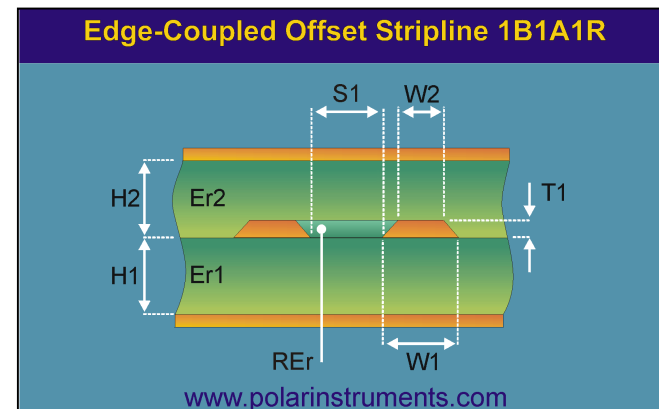
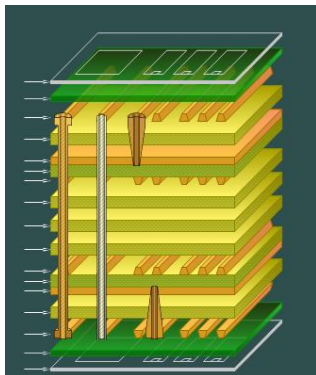
Solder Mask Modelling

- Solder mask has a large effect on impedance on surface traces
- Depending on Geometry can be as large as 5Ω

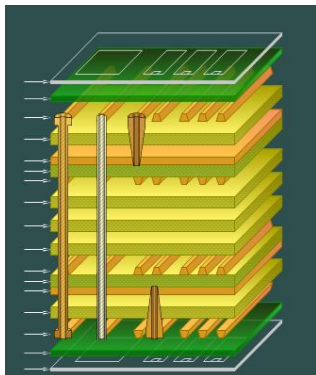
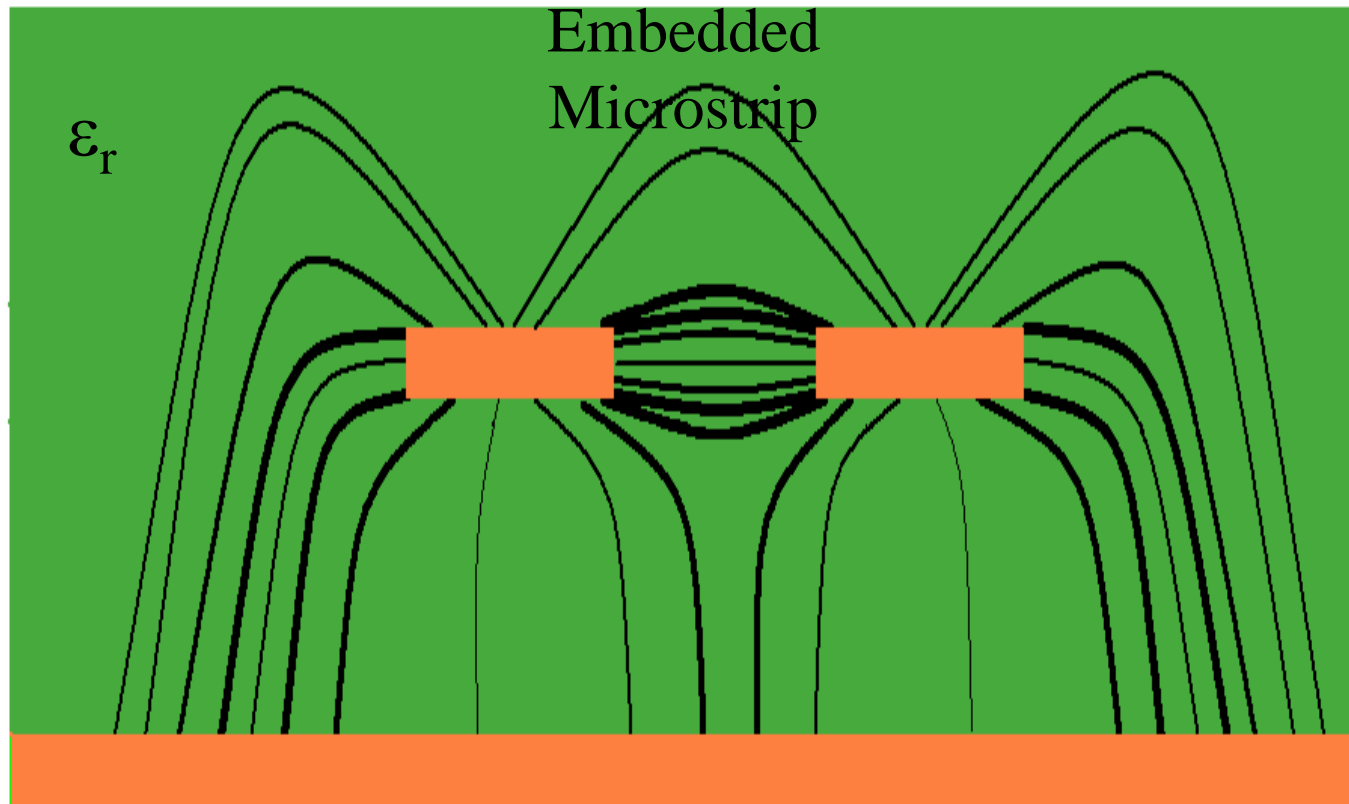


Resign Modeling

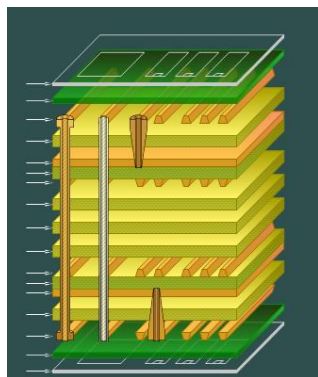
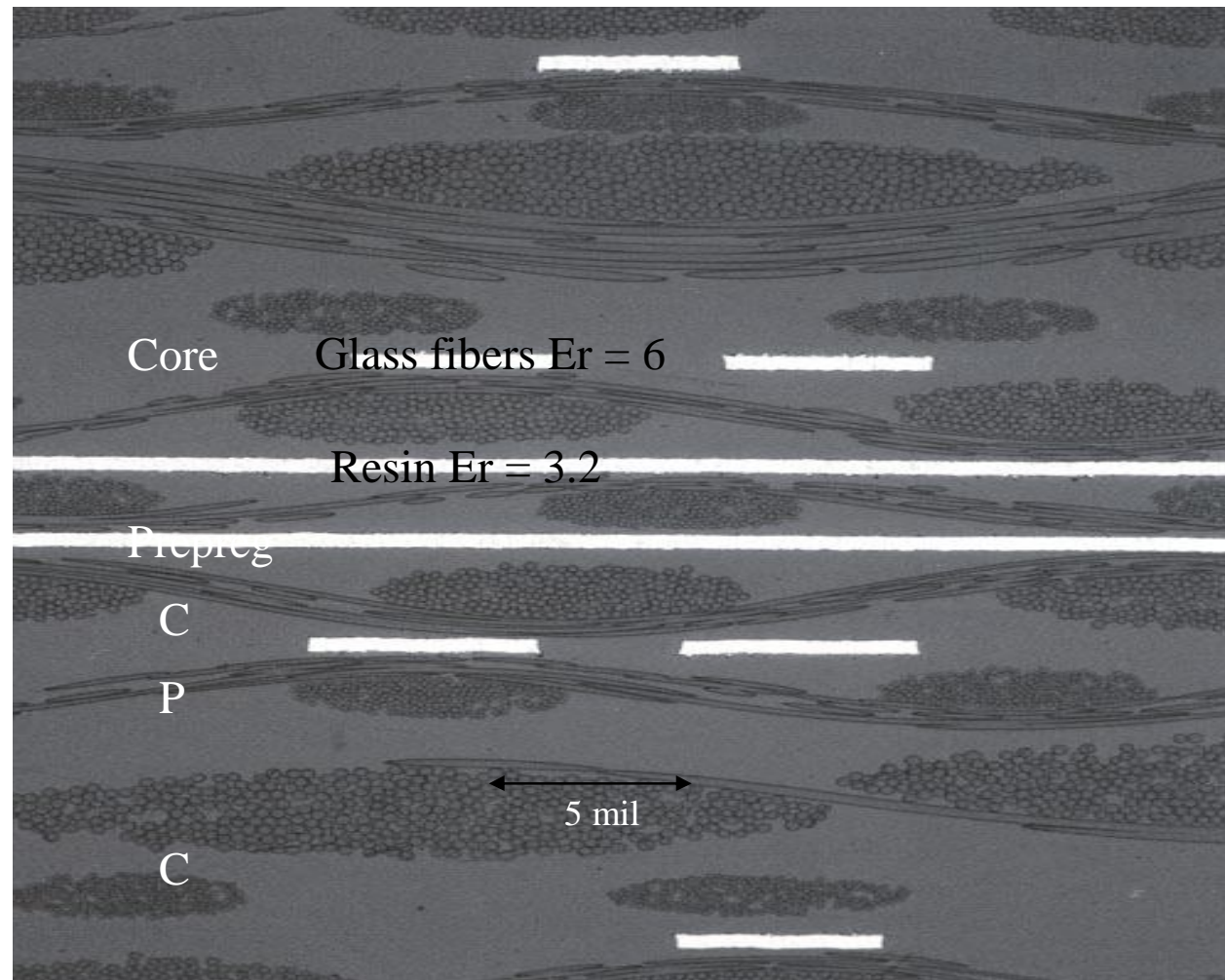
- Both are Mixtures of Resin and Glass Fibers
 - Materials are non-homogenous
 - ϵ_r specified for laminate is the bulk value
 - ϵ_r for glass ~ 6.1 ϵ_r for epoxy ~ 3.2
 - So significant local variations occur for ϵ_r



Typical E-field distribution

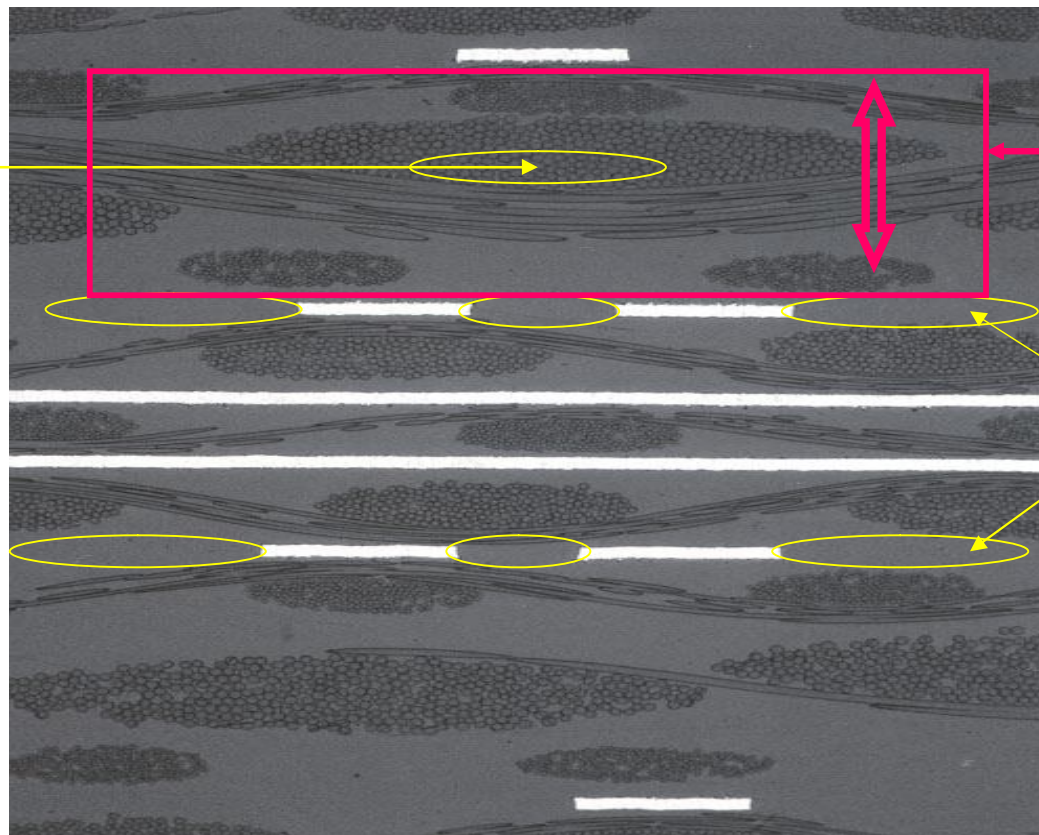
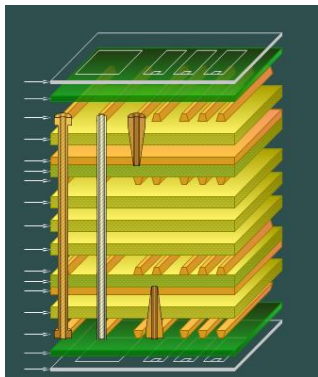


Microphotograph of FR4 structure



FR4 structure

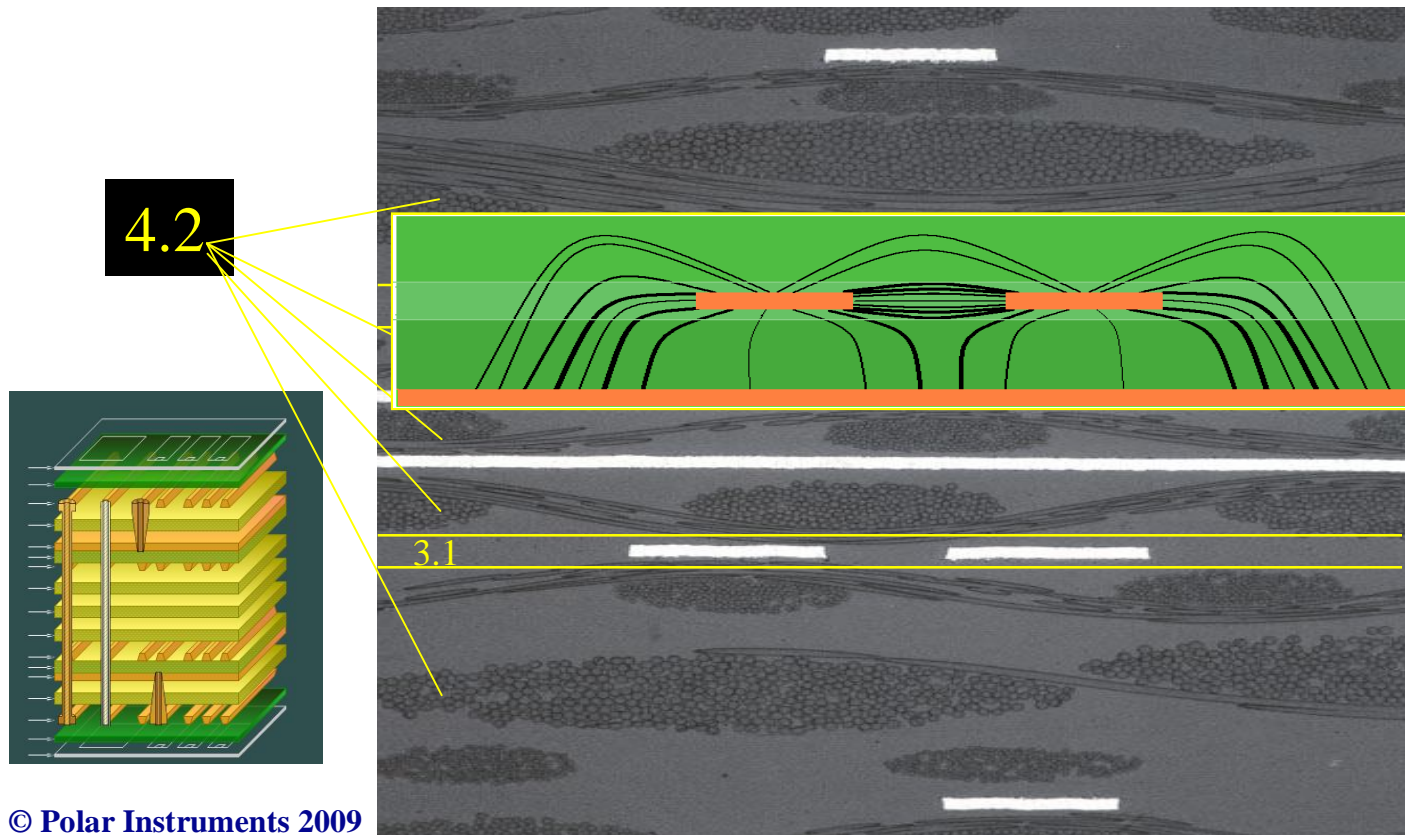
$Er = 6.0$



Bulk Er value in this direction is 4.2 approx

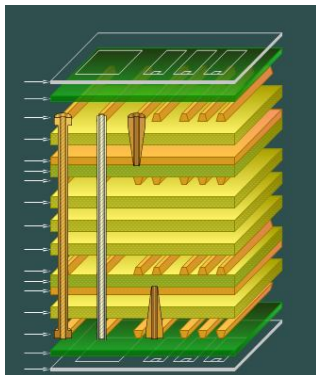
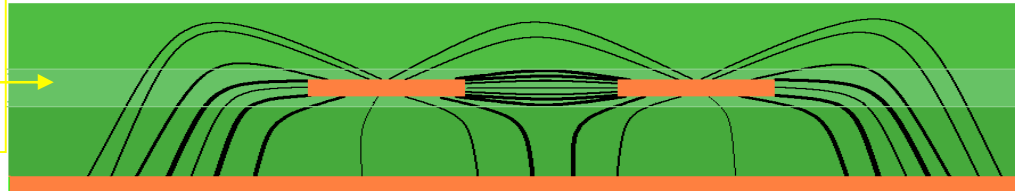
$Er = 3.2$

Field in FR4 structure



Field distribution in Differential Pair

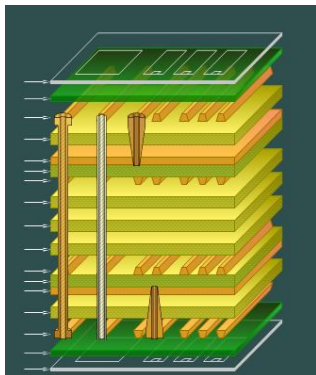
Impedance value
Increases as
Er and C decrease



All Models are Wrong

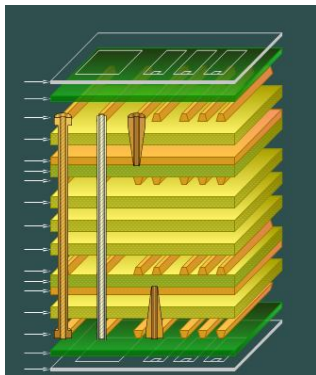
But Some are Useful !!

Tolerance needs to be given on all Simulated results

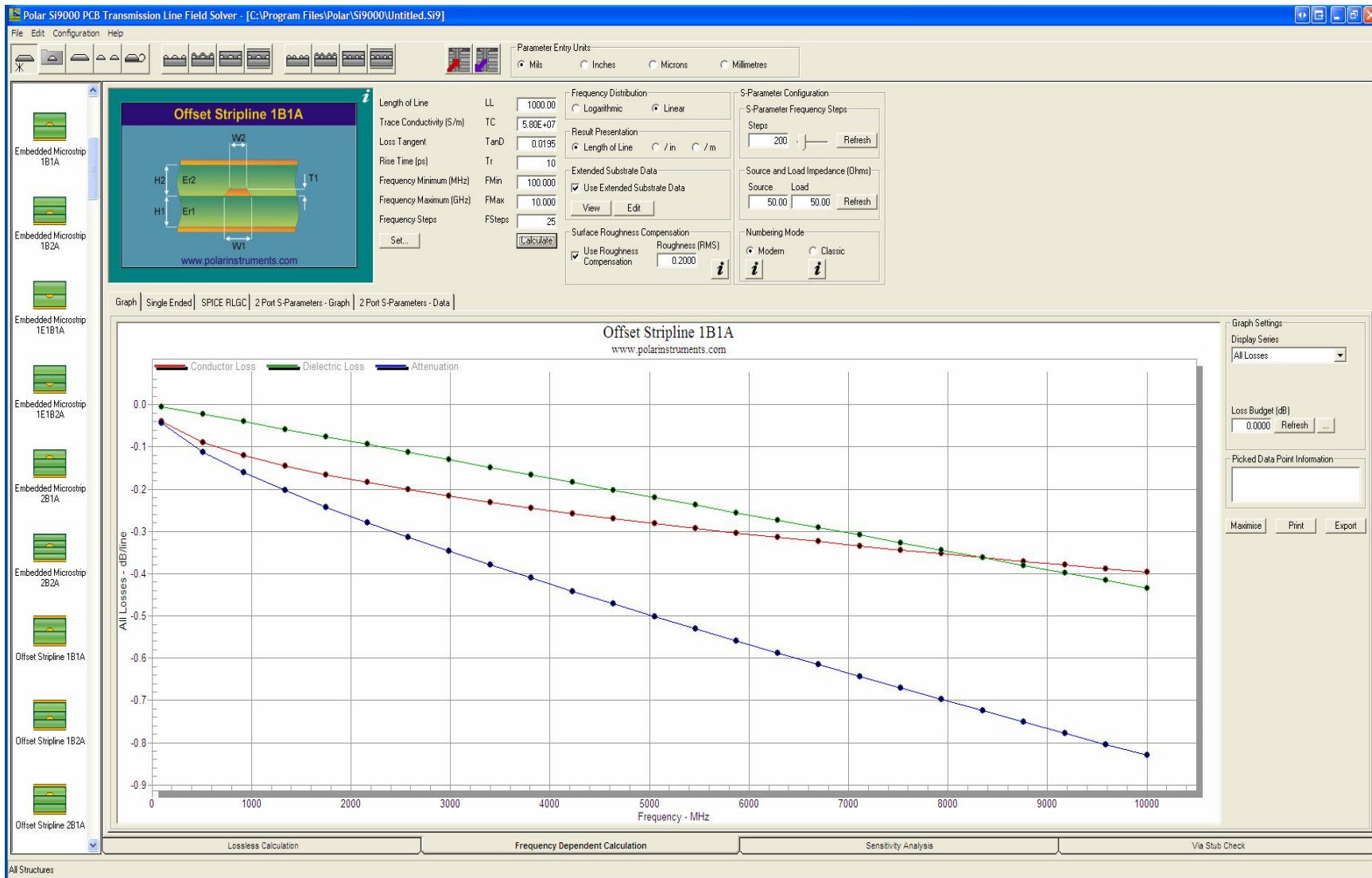


Modelling Losses

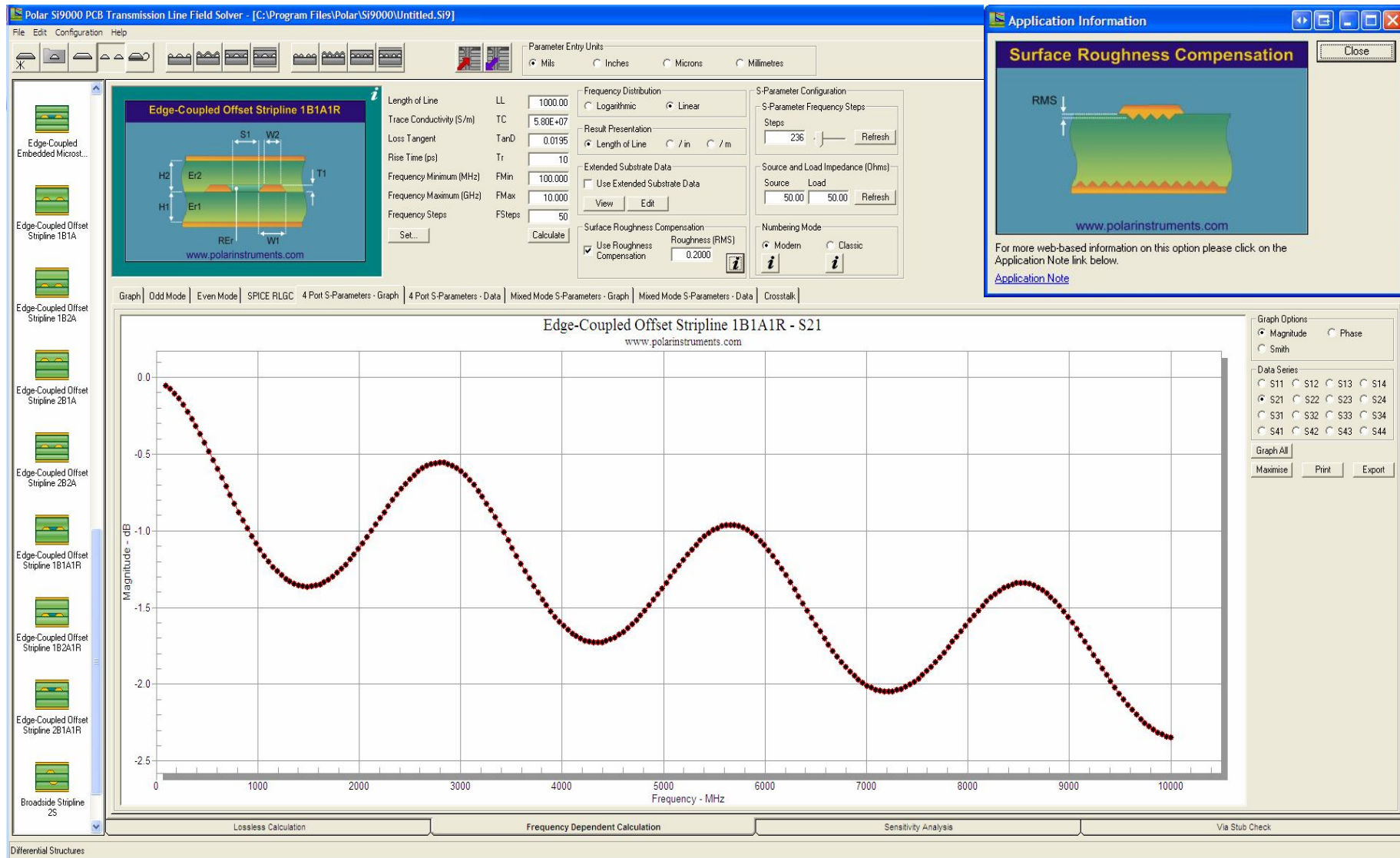
- Designers need to concern themselves with Loss as well as Impedance
- Frequency Dependant Modelling
- Low Dk Material Modelling



Modelling Loss

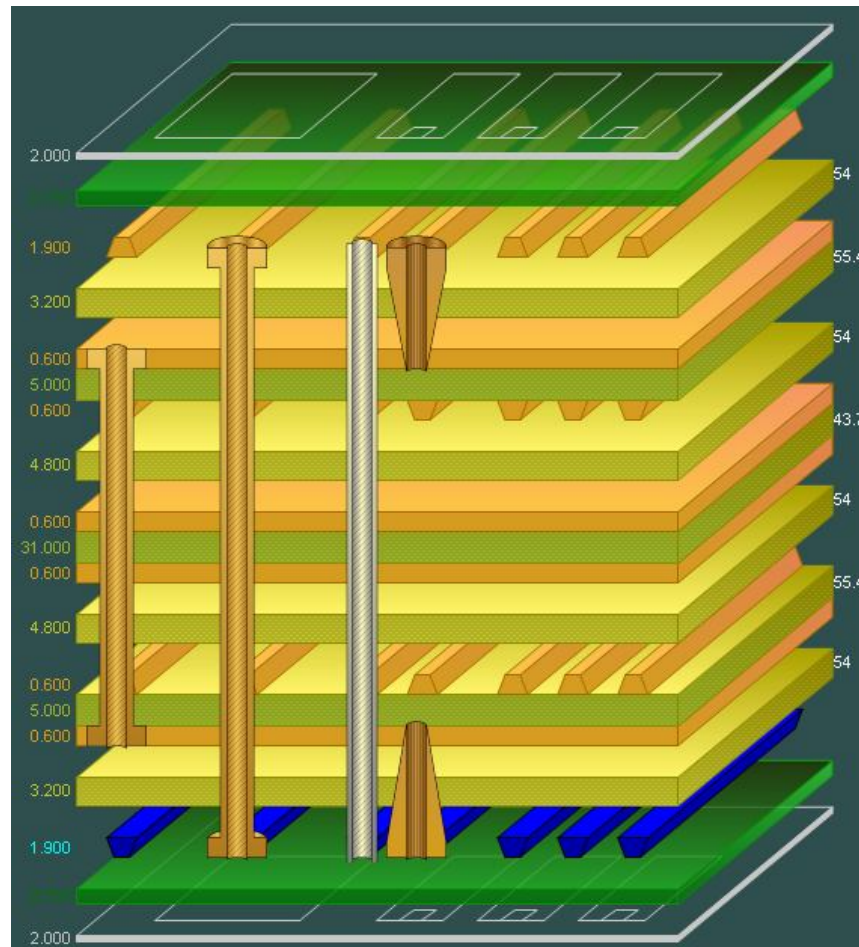
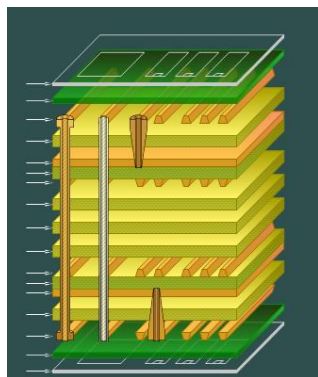


Modelling Loss



So How do we get the modelled results to the fabricator

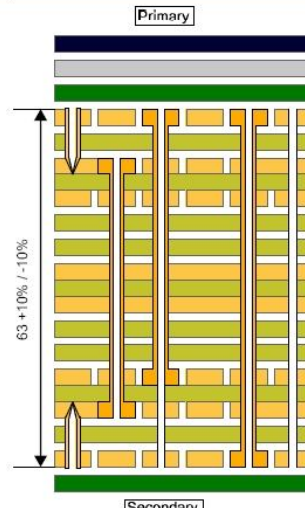
Document your stacks like this:



And like this:



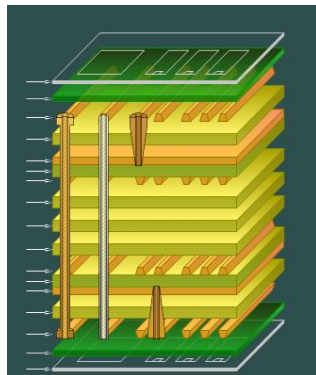
Layer	Stack up	Supplier	Supplier Description	Impedance ID	Description	Processed Thickness	ϵ_r	Data Filenames
Primary								
		Polar Samples	PE/001		Peelable Mask			Primary-Side-Peelable-P1.ger
		Polar Samples	ID/001		Screened Ident			Primary-Side-Ident-I1.ger
		Polar Samples	SM/001		Liquid Photolmageable Mask	4.00		Primary-Side-Solder-Mask-S1.ger
1		Polar Samples	FO/001	1	Copper Foil	1.40		Primary-Side-L1.ger
2		Polar Samples	PP/001		PrePreg 1080	2.79	4.20	
3		Polar Samples	CO/020	2	FR4 Core	1.40	4.20	Ground-Plane/Inner-Tracking-L2.ger
4		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	Inner-Tracking-L3.ger
5		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	
6		Polar Samples	CO/017		FR4 Core	1.40	4.20	3V3-Power-Plane-L4.ger
7		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	1V5/2V5-Power-Plane-L5.ger
8		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	
9		Polar Samples	PP/003		PrePreg 3113	3.44	4.20	Inner-Tracking-L6.ger
10		Polar Samples	CO/020	3	FR4 Core	12.00	4.20	Ground-Plane/Inner-Tracking-L7.ger
11		Polar Samples	PP/001		PrePreg 1080	2.79	4.20	
12		Polar Samples	FO/001	4	Copper Foil	1.40		Secondary-Side-L8.ger
		Polar Samples	SM/001		Liquid Photolmageable Mask	4.00		Secondary-Side-Solder-Mask-S8.ger
Secondary								



Copper Thickness = 11.200 | Dielectric Thickness = 51.340 | Overall Processed Thickness = 62.540

Notes

Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Trace Separation	Ground Strip Separation	Lower Ground Strip Width	Calculated Impedance	Target Impedance	Tol (+/- %)
1	Coated Microstrip 1B	1	2	0	4.25	0.00	0.00	0.00	49.38	50.00	10.00
2	Offset Coplanar Strips 1B1A	3	2	4	19.00	0.00	8.00	15.00	27.84	28.00	10.00
3	Diff Embedded Coplanar Waveguide With Lower Ground 1B1A	7	5	0	12.00	8.50	27.00	0.00	100.57	100.00	10.00
4	Coated Microstrip 1B	8	5	0	20.00	0.00	0.00	0.00	75.30	75.00	10.00

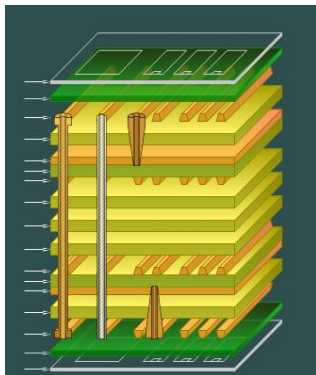
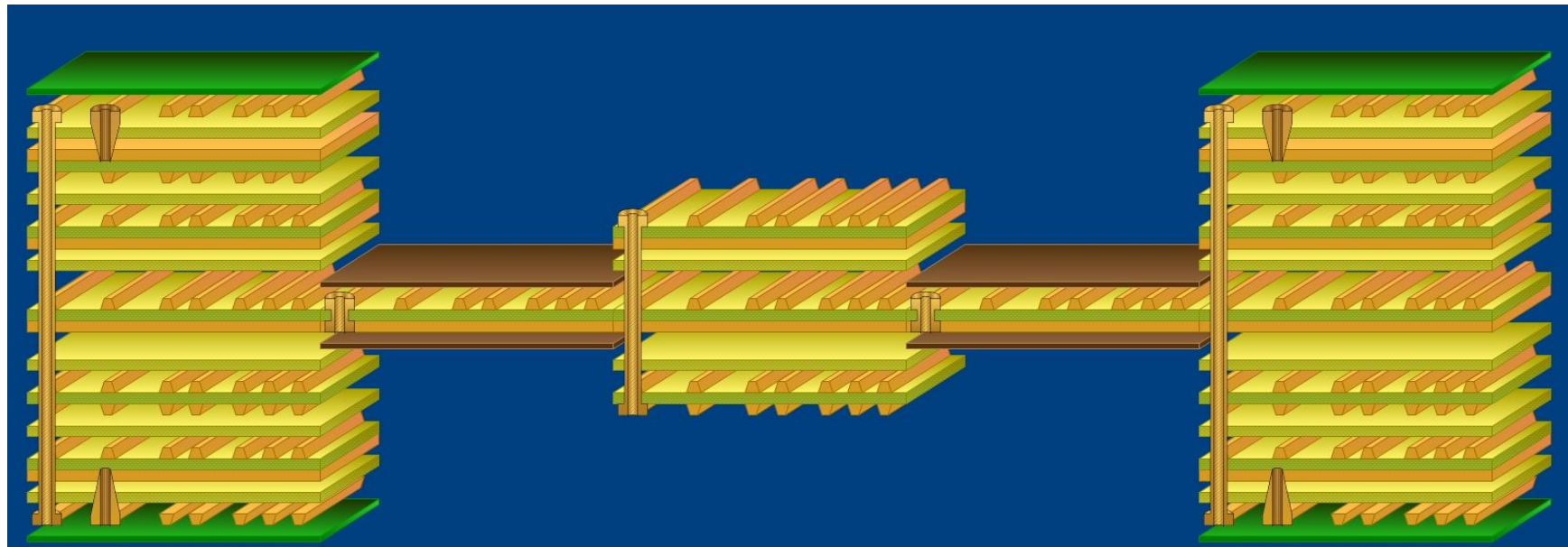


StackName: 8-Layer Sample Stack	Version: A	Revision: 2	Modification: 3113 swp to 108	Date of Revision: 31/3/09	Editor: JAS	Page 1/1	Speedstack 2009
Date: 17/06/2006	Associated Documents:						
Author: James Stapley							
Department: Engineering							
Site: Waterlooville							

Copyright ©

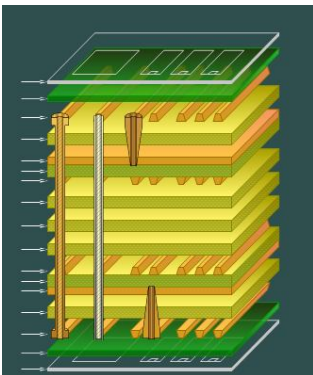
www.polarinstruments.com

Even Document Flex Rigids Like this:



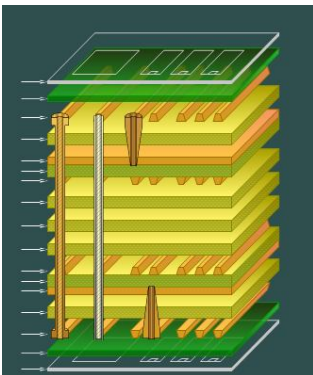
Why is stackup design and communication important?

- Time to market
- Complex designs
- Communication from designer to PCB fabricator
- Increasing impedance requirements
- Can be time consuming
- Good communication saves costly rebuilds



Material Libraries

- Based on the parameters of actual material.
- Separated into material types
 - Cores
 - Prepregs
 - Foils, etc.



The info required for cores

C:\Program Files\Polar\SB200v6\Isola_EU.mlbx

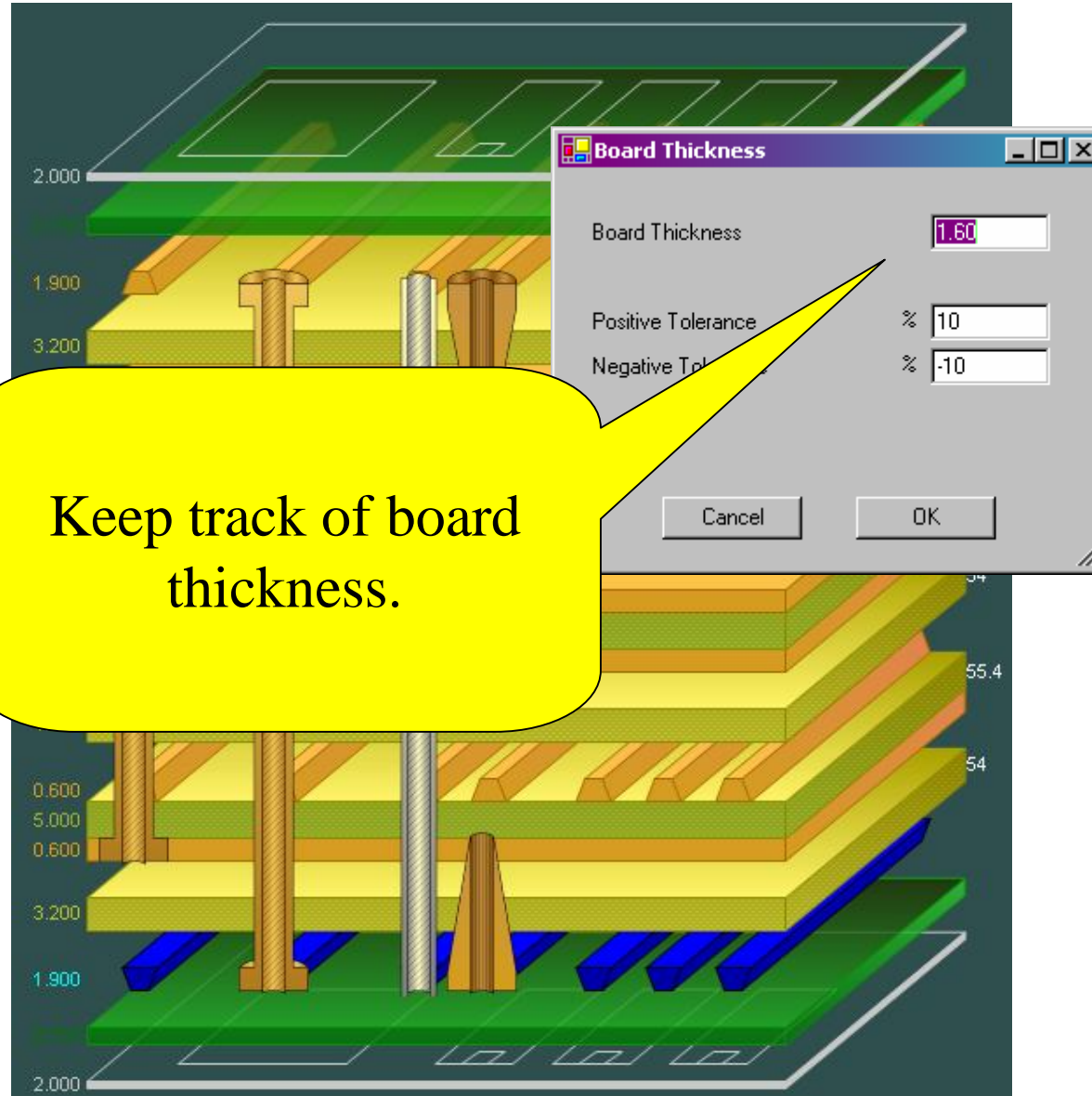
EXIT

Foils Prepregs RCCs Cores Solder Masks Ident Inks Peelable Masks Coverlays

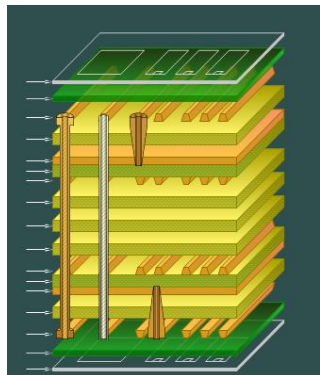
	Supplier	Supplier Description	Description	Stock Number	Dielectric Base Thickness	Dielectric Finished Thidne	Dielectric Constant	Upper Cu Base Thickness	Lower Cu Base Thickness	Resin Content	Tg
	ISOLA	2-2165	De104/TS		0.254	0.254	4.71	0.018	0.018	47.4	140
	ISOLA	2-2165	De104/TS		0.254	0.254	4.71	0.035	0.035	47.4	140
	ISOLA	2-2165	De104/TS		0.254	0.254	4.71	0.07	0.07	47.4	140
	ISOLA	2-2157	De104/TS		0.3048	0.3048	4.72	0.018	0.018	48	140
	ISOLA	2-2157	De104/TS		0.3048	0.3048	4.72	0.035	0.035	48	140
	ISOLA	2-2157	De104/TS		0.3048	0.3048	4.72	0.07	0.07	48	140
	ISOLA	2-7628M	De104/TS		0.3556	0.3556	4.93	0.018	0.018	41.3	140
	ISOLA	2-7628M	De104/TS		0.3556	0.3556	4.93	0.035	0.035	41.3	140
	ISOLA	2-7628M	De104/TS		0.3556	0.3556	4.93	0.07	0.07	41.3	140
	ISOLA	2-7628+1-2125	De104/TS		0.4672	0.4672	4.88	0.018	0.018	44	140
▶	ISOLA	2-7628+1-2125	De104/TS		0.4672	0.4672	4.88	0.035	0.035	44	140
	ISOLA	2-7628+1-2125	De104/TS		0.4672	0.4672	4.88	0.07	0.07	44	140
	ISOLA	3-7628	De104/TS		0.51	0.51	4.96	0.018	0.018	39.6	140
	ISOLA	3-7628	De104/TS		0.51	0.51	4.96	0.035	0.035	39.6	140
	ISOLA	3-7628	De104/TS		0.51	0.51	4.96	0.07	0.07	39.6	140
	ISOLA	3-7628M	De104/TS		0.6096	0.6096	4.78	0.018	0.018	45.3	140

Click on a material row to select it, Double-Click to edit it

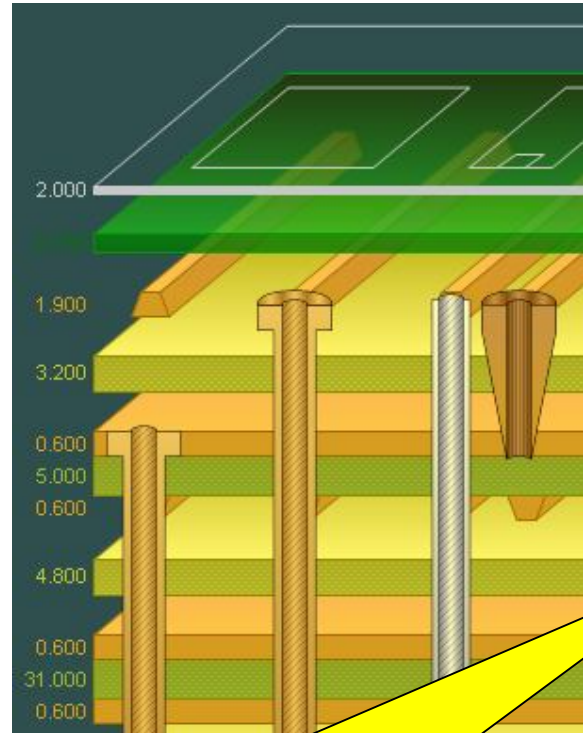
Will it fit?!!



Keep track of board thickness.



D.R.C.



Stack Up Editor DRC : 3 Controlled Impedance

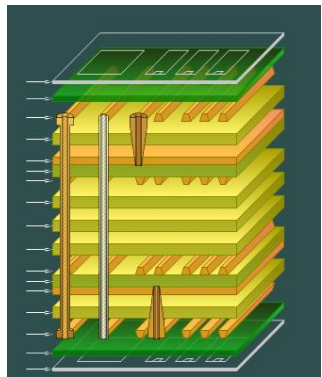
DRC Test Selection

- Design Logic
- Symmetry
- Copper Balance
- Board Thickness
- Manufacturing Tests
 - Min. Trace Width
 - Min. Gap Width
- Aspect Ratios
 - Mechanical Drill
 - Buried Laser Microvia
 - Blind Laser Microvia
 - Trace
 - Excess Resin

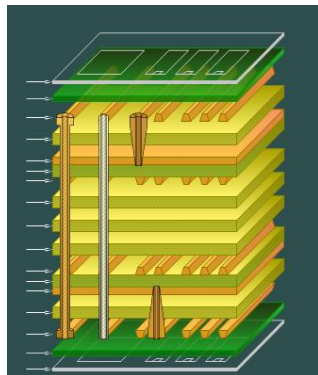
Symmetry : Different Material Types
Symmetry : Different Material Types
Copper not Balanced

Board Thickness

Check that it meets design rules



Adding a controlled impedance structure



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www.polarinstruments.com

Stack Up Editor | DRC : 0 | Controlled Impedance

GS

All | < | > | 1 Of 2

Coated Microstrip 1B

H1, Er1, W1, W2, C2

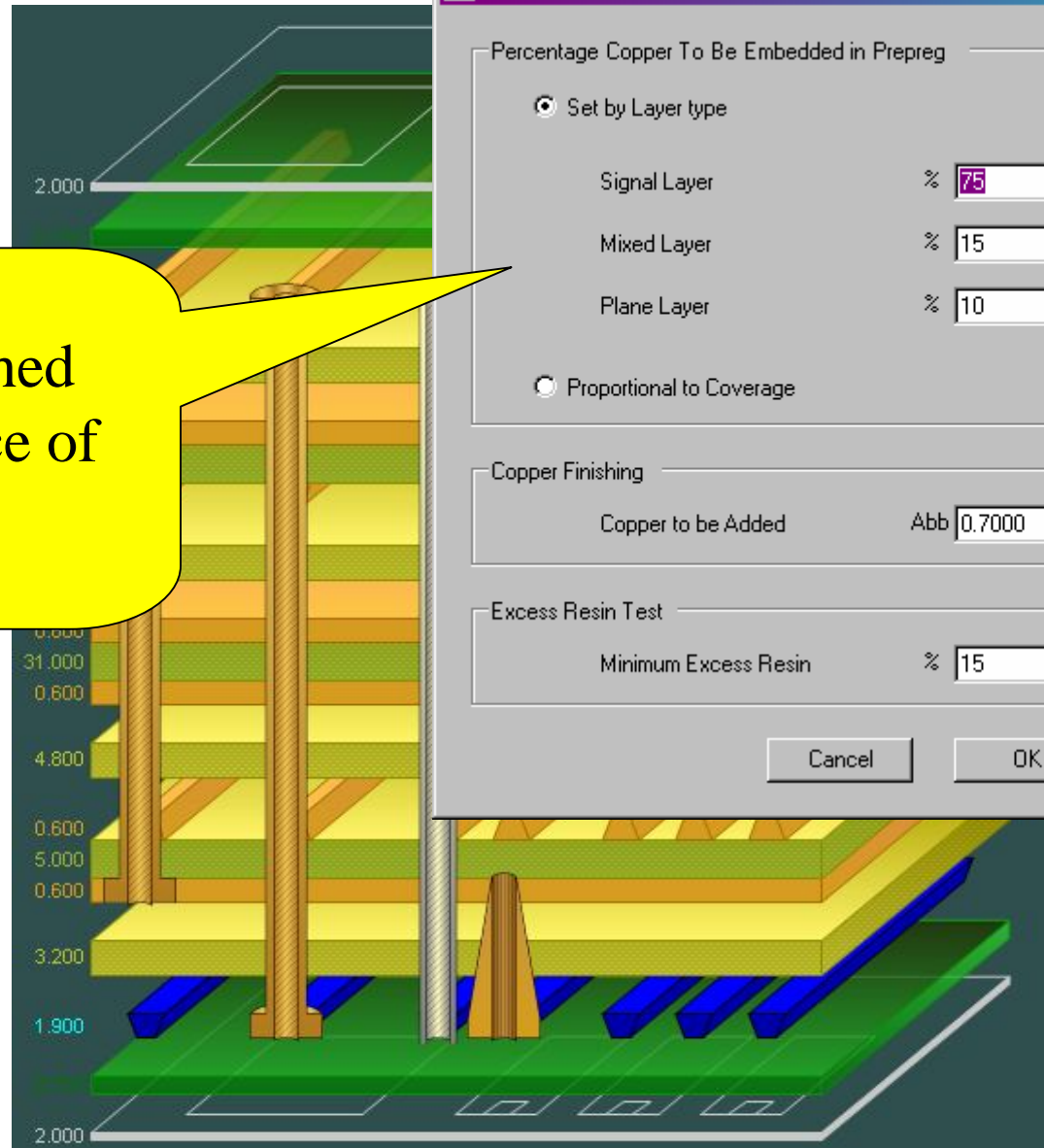
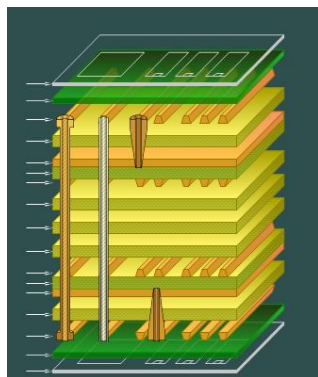
polarinstruments.com

Height	H1	3.2000
Dielectric	Er1	3.9500
Width	W1	5.0000
Width	W2	4.0000
Thickness	T1	1.9000
Substrate	C1	0.7500
Trace	C2	0.7500
Dielectric	CEr	4.1000
Impedance	Zo	50.02
Target Impedance		50.00
Target Tolerance %		5.00

Add a structure on your selected layer

Finished thickness calculation:

Calculate finished thickness (choice of methods).



Prepreg Corrections

Percentage Copper To Be Embedded in Prepreg

Set by Layer type

Signal Layer	%	75
Mixed Layer	%	15
Plane Layer	%	10

Proportional to Coverage

Copper Finishing

Copper to be Added Abb 0.7000

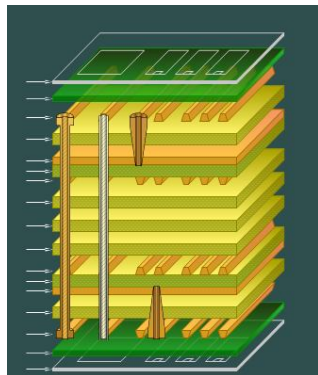
Excess Resin Test

Minimum Excess Resin % 15

Cancel OK

Drill documentation:

Document conventional laser blind buried and stacked vias.



Drill Properties

Electrical Layers

First Electrical Layer No: 1 Trace Column: 4

Second Electrical Layer No: 2

Drill Information

Mechanical

Laser

Through Plated

Data Filenames: []

Hole Information

Hole Count: 1000

Different Hole Sizes: 1

Minimum Hole Size: 0.0060

Apply Close

Coupon Testing

The screenshot displays the Polar Instruments Coupon Generator software interface. The main window is titled "Polar Instruments - Coupon Generator" and shows a "Coupon View" of a rectangular coupon with a complex internal layout of microstrips and vias. The layout is defined by a series of yellow dots forming a border and internal patterns, with a blue line indicating a specific path or boundary.

On the left side, there is a "Stack" table showing the material layers:

Layer	Materials	Type
1		Signal
2		Plane
3		Signal
4		Signal
5		Plane
6		Signal

Below the stack is a "Structures" table:

ID	Name	Target Q	W1
<input checked="" type="checkbox"/>	5	Edge Coupled Coated Microstrip 1B	100 0.508
<input checked="" type="checkbox"/>	6	Edge Coupled Coated Microstrip 1B	100 0.508

At the bottom of the main window, the following information is displayed:

Mouse [106.147, -3.078]
Zoom [178.2 %]
Rotation [0.0 °]
Units [millimeter]
Coupon Surface Area [7112 mm²]

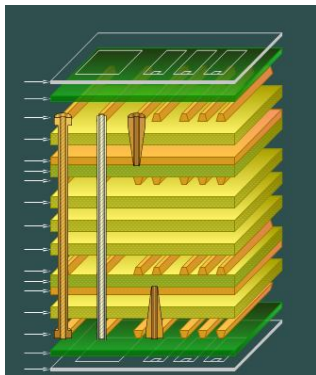
TDR Testing



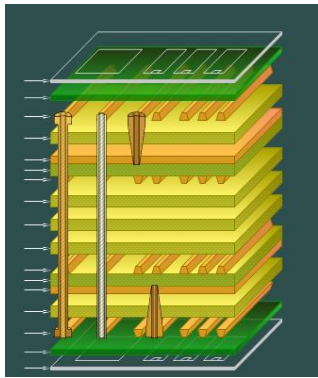
- Testing is not difficult or Time consuming
- Required for Process conformance to Specification.
- MVT not DVT.

The Future of testing:- Atlas

- New high speed busses in Multi GHz range
 - SuperSpeed USB 3.0
 - PCI Express Gen 2.0
- Differential Signalling techniques allow the continued uses of FR4
- Requires accurate control of transmission line losses



The Future of testing:- Atlas



Atlas Coupon Test

Polar Instruments - CGen Coupon Generator - [polar_set2dil MWP1585.cxf]

File Tools Coupon View Options Help

Millimetre POLAR INSTRUMENTS SET2DIL MWP1585

Stack

Layer	Materials	Type
1		Signal
2		Plane
3		Signal
4		Signal
5		Plane
6		Signal

Coupon View

Structures

ID	Name	Target Ω	W1	S1
<input type="checkbox"/>	Edge Coupled Coated Microstrip 1B	85	0.23	0.3
<input checked="" type="checkbox"/>	Edge Coupled Coated Microstrip 1B	100	0.17	0.33
<input checked="" type="checkbox"/>	Coated Microstrip 1B	50	0.188	0

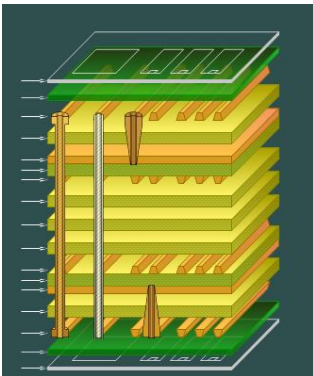
1: L1 85 Ω (W1=0.23 S1=0.3) 4: L4 85 Ω (W1=0.245 S1=0.25) 7: L4 50 Ω (W1=0.225)
2: L1 100 Ω (W1=0.17 S1=0.33) 5: L4 100 Ω (W1=0.182 S1=0.318) 8: L6 50 Ω (W1=0.188)
3: L1 50 Ω (W1=0.188) 6: L4 50 Ω (W1=0.225) 9: L1 REFERENCE

Mouse [144.823 , 67.199] Mixed Layer Mode [Plane]
Zoom [220.1 %] Coupon Style [Style POLAR SET2DIL]
Rotation [0.0 °] Layer [1]
Units [millimeter]
Coupon Surface Area [5806.441 mm²]

Errors

Conclusion

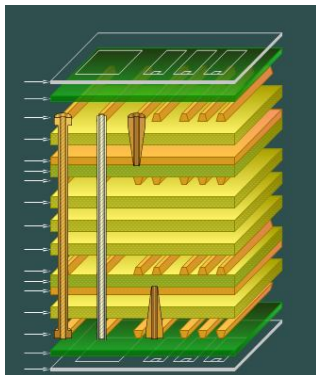
- Accurate Modelling is as important as final testing.
- Material selection is critical to the performance of the final product
- Clear Documentation is imperative
- Testing final product is made easy through robust test system.



Thank You

- Questions?.....

Neil@polarinstruments.com



www.polarinstruments.com