

# **Future Trends and UK Research in Interconnect Technology**

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# The Innovative Electronics Manufacturing Research Centre (IeMRC)

- Established in 2005
- Allocated £5 million to support research in UK academia
- Strong industrial input in setting research agenda
- Currently supporting more than 30 projects
- Most projects have a significant industrial input



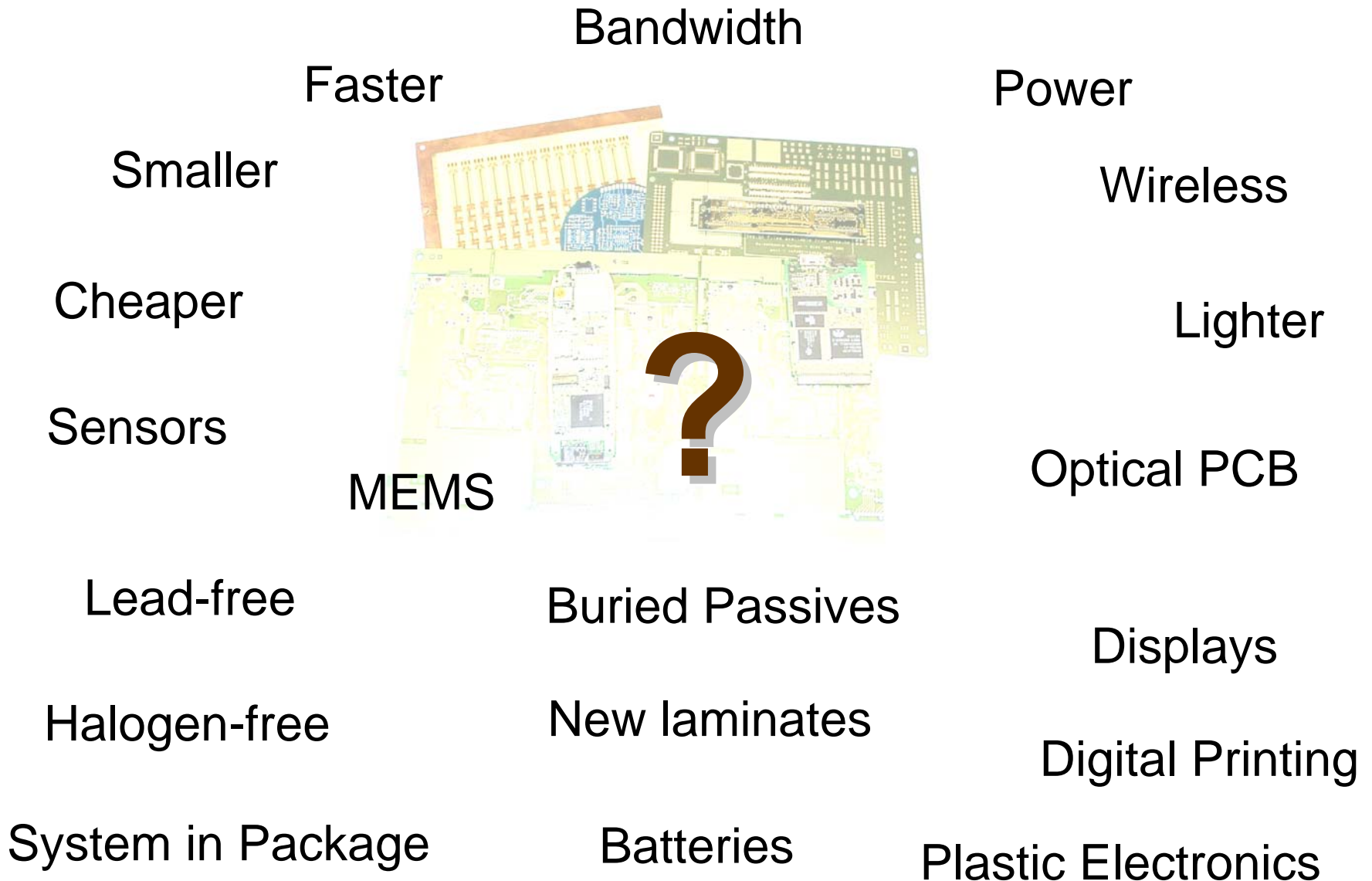
# The IeMRC Mission

To establish a 'Centre of Expertise' through which UK  
industry can access and influence research in electronics  
manufacturing

**Supporting UK research on Advanced Interconnection**



# Future Trends in Interconnect Technology



# Interconnection Driven by Device Technology

- Semiconductors are at the 63 nm node and moving to 45 nm
- Intel has designed a CMOS transistor that is 30 nm across its base
- 10 GHz devices with billions of transistors by 2010
- Devices with more functionality, higher speed, more processing power
- Demand for new ways of packaging and interconnecting them

**DEVICE** → **PACKAGE** → **INTERCONNECT**

# Challenges for PCBs

- To provide interconnects for increasingly complex devices and their packages
  - greater numbers of I/Os
  - higher operating frequencies, signal integrity
  - broader bandwidth
  - environmental compliance ie lead-free and halogen-free
  - many potential technology solutions



# Possible Solutions

- Buried passives – integrate passive components into the PCB structure
- Optical interconnect for high speed, data-rich signals
- Buried waveguides, chip to chip optical links, optical backplanes
- New types of packaging - the emergence of System in Package
- Printed electronics, plastic electronics, nano.....
- Plus many other individual tailored solutions for specific applications

# Materials for Future Interconnects

- There are many materials challenges for future interconnects
- New laminates – better thermal stability, reduced thermal expansion, improved dielectric properties, lead-free compatibility, halogen-free
- New polymers for waveguides - thermally stable polymers with low propagation losses
- High dielectric constant materials
- Improved metallurgical properties

# Embedding Passives in the PCB

- Replaces surface passives with buried passives
- Frees up the board surface
- Established technology with various processes
- Useful for some applications eg mobile phones

## **BUT**

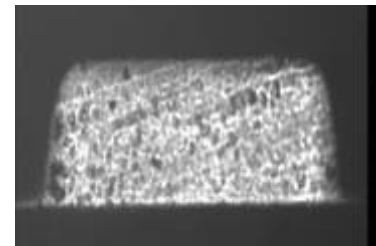
- Buried passives have fixed overhead and material costs
- Design, test and reliability implications
- Why not put the passives near the devices eg in the package?

# Integrated Devices – Further Options

- Integrate active devices into the board
- Integrate into a separate structure
- Move passives into package
- System in Package can accommodate  
this type of approach
- Individual solutions being developed

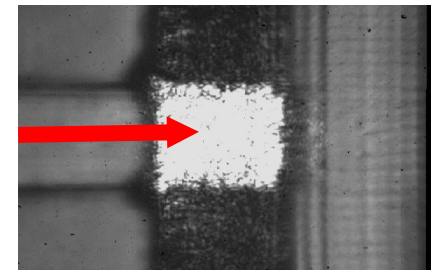
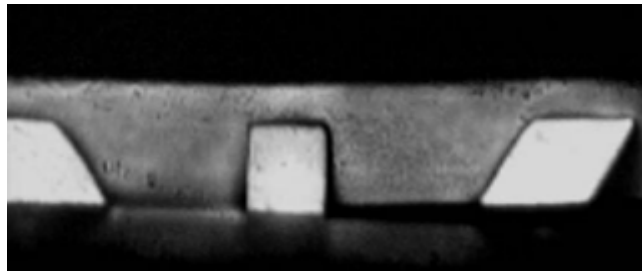
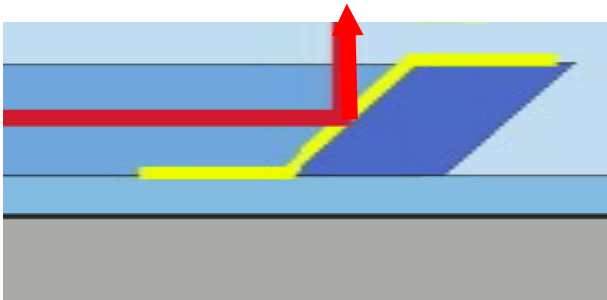
# Embedded Waveguides

- Conventional metal conductors present a problem as microprocessor speeds move into the Gigahertz region
- Optical interconnection can provide a solution for high speed interconnects between devices or even boards
- Fully embedding waveguides into the PCB provides one solution
- Encouraged by the availability of VCSELs and photodiodes and the emergence of thermally stable polymer waveguide materials
- A major area of support for the IeMRC



# leMRC Opto-PCB Flagship

- Integration of optical waveguides with printed circuit boards
- Integrated optical and electrical interconnected PCB (OPCB) for backplanes and daughter cards
- High bit rate (10 Gb/s), error-free, reliable, dense connections
- Project undertaken by UCL, Loughborough, and Heriot-Watt with 9 industrial partners including NPL, Stevenage and BAe



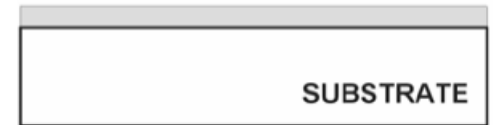
# leMRC Opto-PCB Flagship

- Establish waveguide design rules
  - build into commercial CAD layout software to ease the design of OPCBs and to ensure widespread use
  - understand the effect of waveguide wall roughness and cross sectional shape on loss and bit error rate
- Develop low cost, PCB compatible, manufacturing techniques for OPCBs
  - compare the commercial and technological benefits of several high and low risk manufacturing technologies
  - carry out environmental testing, reproducibility
- Design an optical-electrical connector
  - low cost, dismountable, passive, self-aligning, mid-board, multichannel, duplex, long life

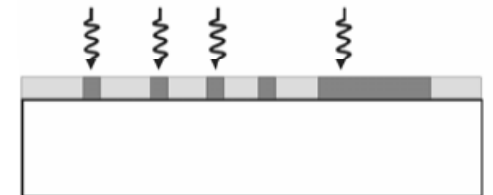
# leMRC Opto-PCB Flagship

- Ink jet for localised deposition of waveguides and cladding
- Excimer laser ablation of waveguide structures
- Direct laser writing of waveguides
- Investigating formation of profiled mirrors and subsequent metallisation
- Self alignment of lasers and detectors with waveguides

1: APPLY POLYMER TO SUBSTRATE



2: LASER WRITE STRUCTURES



3: DEVELOP POLYMER

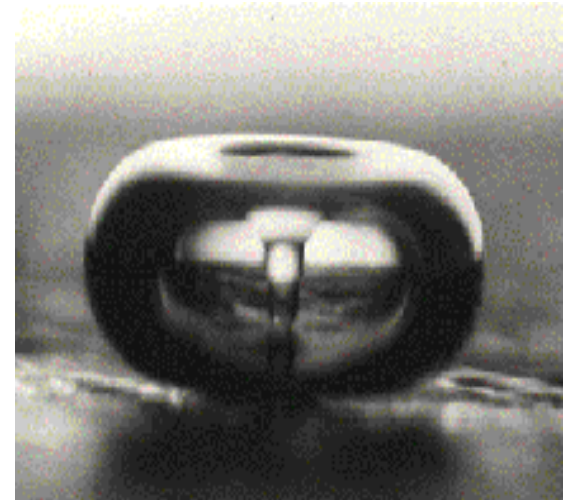


# Sonochemistry Research at Coventry

- Good adhesion is required at many interfaces used in electronics interconnect manufacturing, eg metals on polymers
- This is typically achieved by the use of aggressive and environmentally undesirable chemical processes
- An alternative method being developed at Coventry is to use sonochemical routes to offer more benign processes
- Use of ultrasonics can reduce process temperatures and generate less waste etc

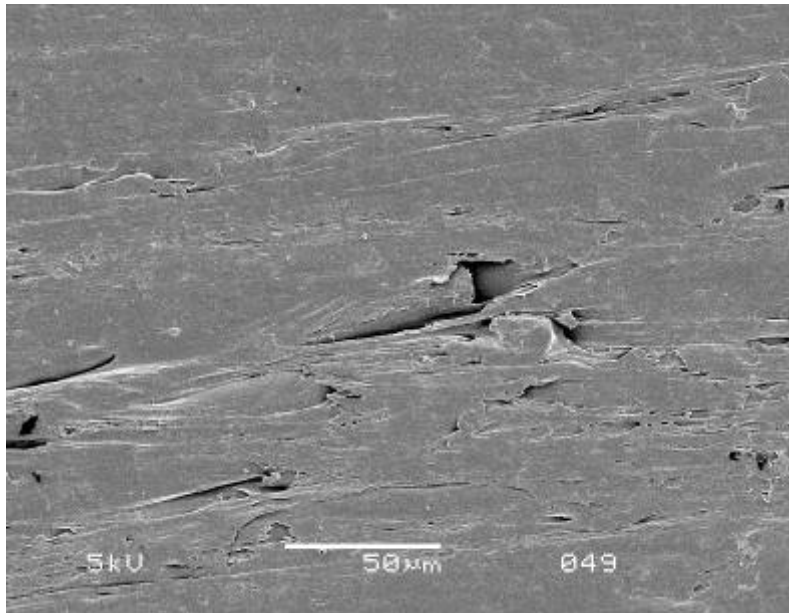
# Acoustic Cavitation - the Driving Force for Sonochemical Surface Modification

- **Microjetting**
  - mechanical/physical attack of surface
  - scrubbing/cleaning action
  - destruction of boundary layers
  - movement of reactants to, and products away from, the surface
- **Extreme temperatures and pressures**
  - chemical/oxidative attack of the surface due to oxidative species
  - breaking of bonds on surface of material
  - chemical reactions on surface

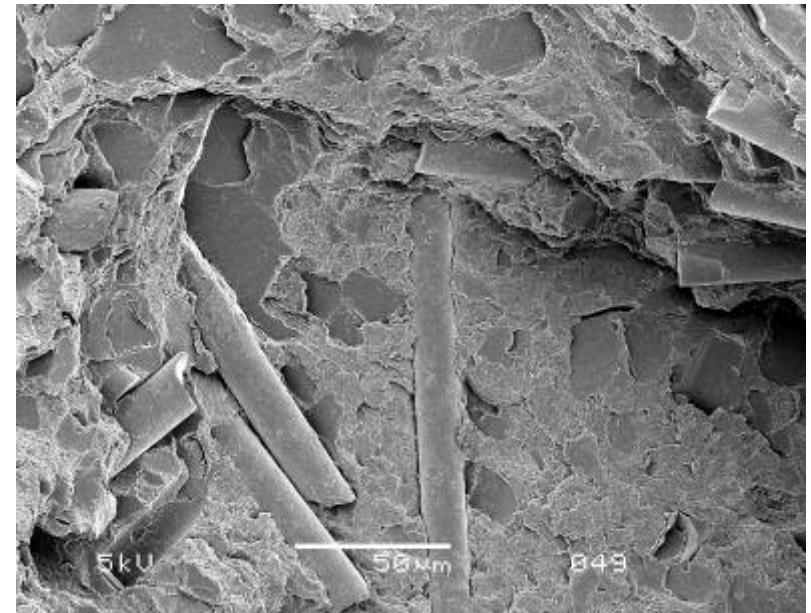


# Texturing the Surface of Noryl (PPO)

**Silent**



**20 kHz Ultrasonic Probe**

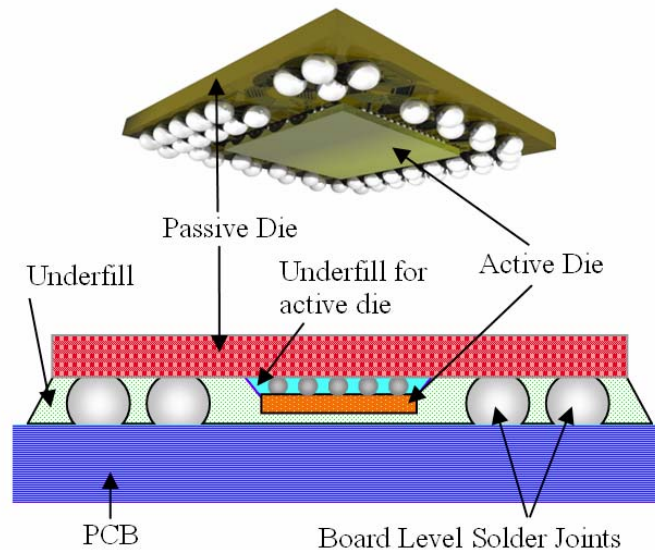


**Noryl samples textured in DI Water (40°C for 60 minutes)**

**Magnification x 500**

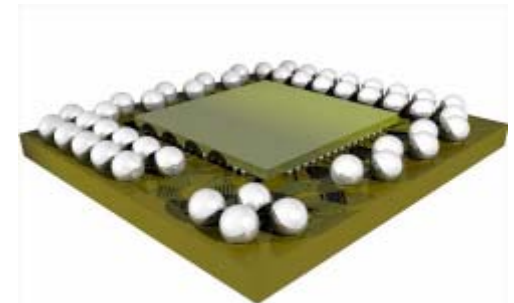
# System in Package (SiP)

The integration of several Integrated Circuits and components of various technologies (RF, analogue, digital, Si, GaAs) in a single package, resulting in one or several electronic systems



# leMRC SiP Project

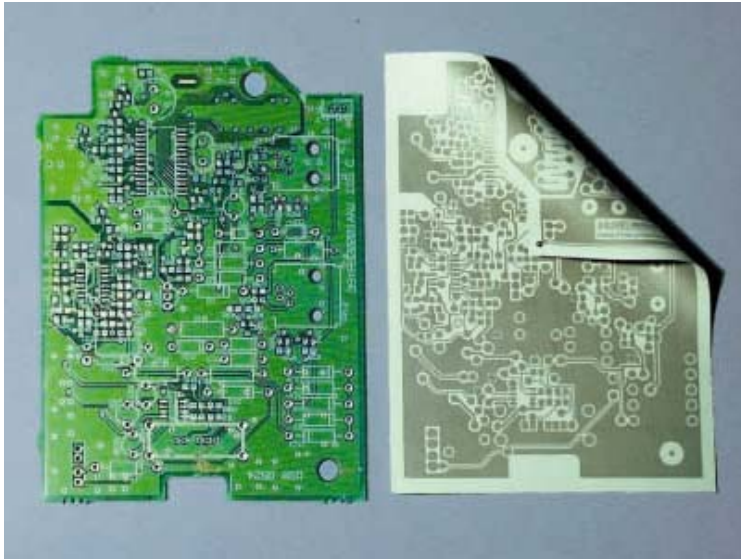
- Lancaster and Greenwich Universities plus industrial partners
- Design for Manufacture Methodology for SiP
- Reliability Engineering of SiP assemblies
- Solder ball and assembly reliability modelling
- Embedded test and reliability indicators
- See leMRC website for more details



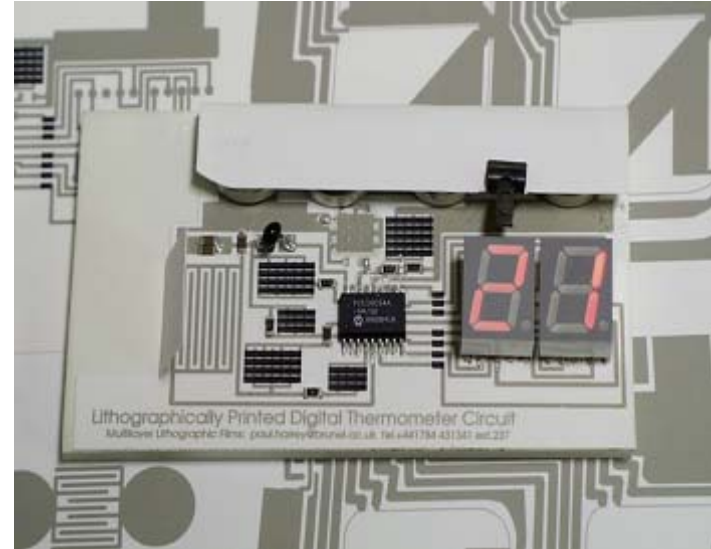
# Printed Electronics at Brunel

The "Conductive Lithographic Film" (CLF) circuit fabrication process is a method of forming electronic circuit interconnect and components on flexible substrates via use of the offset lithographic printing process

# CLF Demonstration Circuit



- Landline telephone mainboard
- Artwork taken from original resin laminate circuit board
- SMT passive components attached using conductive adhesive



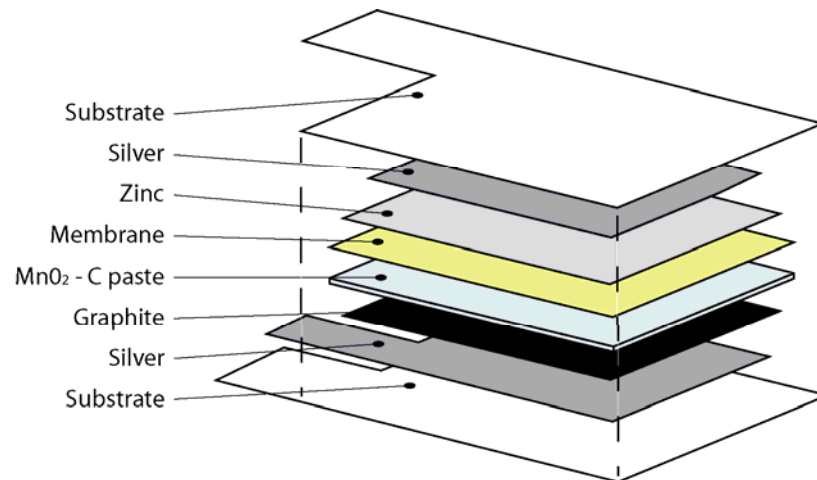
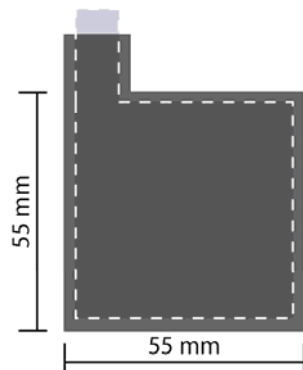
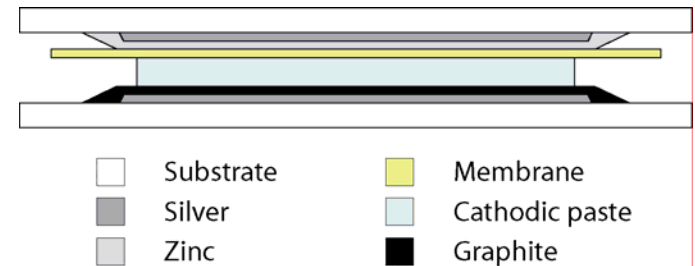
- Microprocessor controlled thermometer
- Circuit interconnect, resistors, capacitors and switch actuator, all printed by offset lithography
- Device uses a glazed paper as the circuit substrate

# Printed Battery Cell Structures

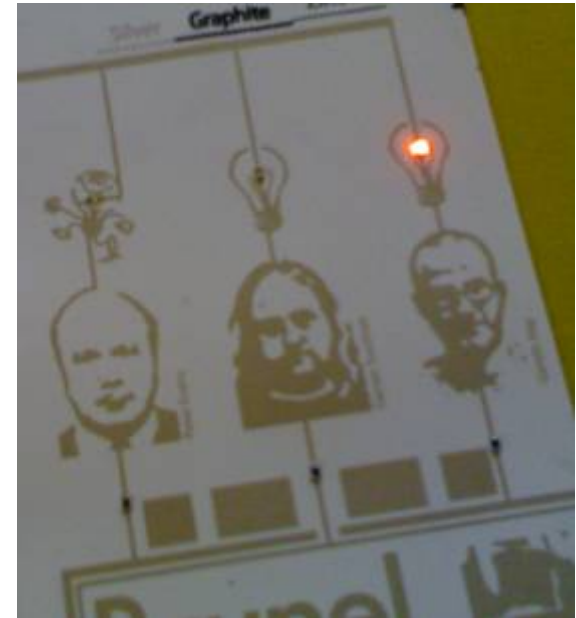
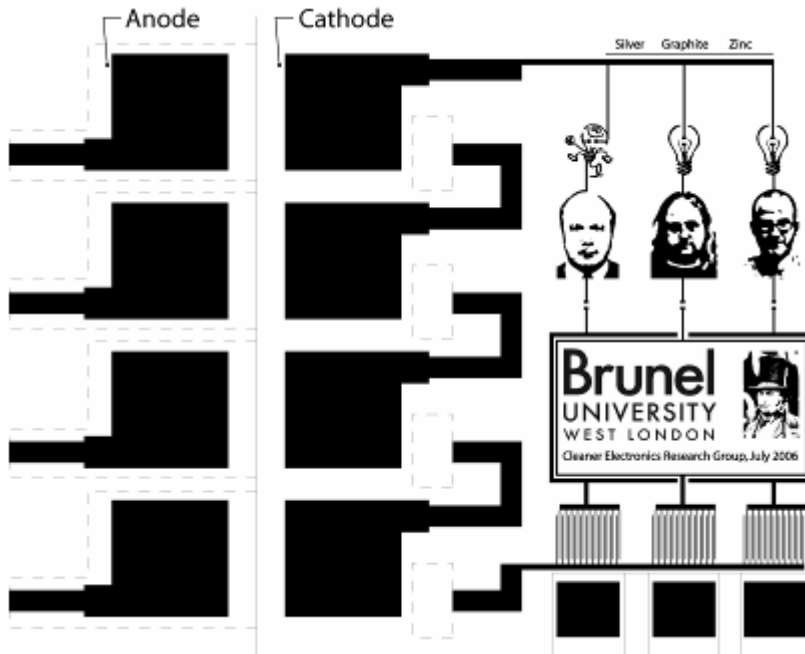
Printed on a non-porous substrate material

Use silver current collectors

Manganese dioxide



# Printed Battery Demonstrator Circuits



Demonstrator printed on 'PolyArt' substrate material

Includes four cells producing a potential of 6.0 to 6.5V

Incorporates printed switch pads

Surface mount LEDs and resistors attached with conductive adhesive

# Further into the Future – Nanoconnections

- Carbon Nano-Tubes (CNTs)
- Potential to form very small conductors
- CNTs also exhibit novel features
- Exceptional electrical and mechanical properties
- Carry high currents with no heating of the CNT
- IeMRC programme to develop conductive, optically transparent materials using CNTs

# Integrated Functionality in PCBs

- PCBs will no longer simply provide electrical interconnects
- They may also include optical wave guides and/or MEMs
- Specialised boards may contain elements of all three approaches
- Combinations of electrical, optical and mechanical functions
- Interesting interconnect challenges for this multifunctionality

# Summary

- Feature sizes are continuing to get smaller and functionality is increasing – this will continue
- We are at the point where new generations of device packaging are emerging eg SiP
- These require increasingly advanced interconnect approaches
- There is a growing fragmentation of possible solutions at the leading edge of interconnect technology

# leMRC Interconnect Projects

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